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Full bridge converter with reduced voltage stress and zero-voltage switching for LED based lighting application

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ABSTRACT

Light emitting diodes (LEDs) have emerged as an energy efficient lighting source in lighting industry. However, LEDs are current controlled devices and they require efficient driver circuits to illuminate uniformly. This research work presents a full bridge-based converter to drive multiple LED lamps. In the proposed topology, two different direct current (DC) input sources are connected in anti-series across the full bridge, which significantly reduces voltage stress on the switches. Zero-voltage switching (ZVS) is achieved using a single inductor, which minimizes switching losses and improves efficiency. The converter powers three LED lamps, in which two are identical lamps. In each leg of full bridge configuration, two inductors with different current magnitudes are connected to diminish current stress of conducting device. Additional advantages include low power processing, high efficiency, pulse-width modulation (PWM) dimming, driving multiple lamps, and reduced component count. A detailed theoretical analysis of the converter's operating modes is provided to explain its performance and behavior. The concept is validated using numerical simulations with a total power rating of 60 W to validate the steady-state operation.

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1. INTRODUCTION

The efficient use of energy resources has been significantly supported by the adoption of light emitting diodes (LEDs) as an energy efficient light source in the global lighting sector [1]. LEDs have significant features: i) they offer greater energy efficiency, ii) they are environmentally friendly as they do not emit toxic gases, iii) they possess a long operating lifespan, iv) they provide high lumen per watt feature, and v) they exhibit an excellent colour rendering index [2]. LEDs voltage-current characteristics are equivalent to those of the Shockley diode, exhibit an exponential increase in current with small forward voltage changes. Such variations can potentially harm the LED or influence its brightness. Therefore, an LED driver is essential to provide a steady current to the LEDs [3].

LED lighting systems are powered either from direct current (DC) supply or alternating current (AC) supply systems. However, there has been an increased focus on DC-fed LED drivers in recent times, particularly for applications powered by batteries or solar energy [4]. Soft-switching DC-DC converters in high-power LED applications enhance efficiency at higher operating frequencies and achieve improved power densities [5], [6]. A soft switching boost converter [7] is introduced for LED driver applications, demonstrating a 6% improvement in efficiency over a conventional converter.

In the research work [8], a buck and boost operated converter utilizing multi-phasing is proposed. In this study, magnetic core size is reduced and magnetizing current is used to discharge parasitic capacitance of the switches. An interleaved flyback converter introduced in [9] offers isolation between the power supply and the load, enabling this driver to effectively power high-power LED loads. Multi-resonant DC-DC configurations are presented in [10]-[14] to drive multiple LED strings with high energy efficiency and independent dimming control. However, multi-resonant topologies increase complexity of LED systems.

The full bridge-based LED driver topologies given in [15]-[20] are capable of powering multiple loads while minimizing the number of components required, achieving high efficiency through soft switching across all semiconductor devices. A full bridge converter is presented in [15] to power four LED lamps simultaneously. Zero-voltage switching (ZVS) is obtained using a single inductor and lamp current regulation is incorporated using converter input voltage control. An input voltage-controlled full-bridge inverter LED driver is introduced [16]. A double-ended forward converter (DEFC) is employed alongside the full-bridge inverter to regulate the inverter's input voltage in response to supply voltage variations. Alonso *et al.* [17] have explained a variable inductor (VI) based LED driver circuit for DC grid lighting applications. This driver uses a half-bridge inverter, a VI and a center tapped diode rectifier. Both regulation against input voltage and load variations and dimming operations are accomplished through VI. To design a VI, it requires an auxiliary winding with a driver which changes the magnetic flux density in magnetic core material. This VI based LED driver offers an efficiency of 85% at full illumination level. A driver circuit [18] based on switch-controlled capacitors (SCCs) is suggested for multi-channel LED current balancing applications. However, peak currents in switched capacitor LED drivers are significant. The resonant LED driver in [19] provides output current regulation over a wide input voltage range. However, it is suitable for single-load low-power applications. A resonant LED converter is presented in [20] and its features are wide input voltage range, high efficiency, soft switching characteristic, and complete current regulation. However, increased component count and control circuit complexity are its key limitations.

The converter circuits for multiple LED based lighting systems are discussed in [21]-[25], featuring soft switching and dimming control features. A converter topology using three legs, is introduced in [21] to power two LED bulbs with differing power ratings. This topology employs phase modulation for regulating high wattage lamp and asymmetric duty ratio control for regulating low wattage lamp. Partial ZVS in first leg of the configuration is reported. Two half bridge-based resonant converters are realized using three switches to power two LED loads independently [22]. Component count per lamp is very low, but the implementation of control logic is complex. A novel resonant converter is presented to power to multiple LED loads with variable output gain [23]. Variable operating frequency control is employed to regulate LED illumination. The scalability of the converter increases component count per lamp.

A soft-switched full bridge-based LED driver is proposed in [24]. It powers multiple LED lamps, providing several benefits including low switch conduction losses, lamp currents with low ripple, soft switching, enhanced power efficiency, and input regulation. A three-leg soft-switched converter [25] to supply two lamps with independent dimming control is proposed. Two output voltages are generated using two input buck operation to power two similar wattage lamps. However, the current stress is not equal for all switches.

This research paper presents a full bridge LED driver configuration that utilizes two input voltages. The two input voltages are arranged in an anti-series configuration, and their difference acts as the input voltage for the full bridge. The proposed LED driver offers several advantages, including the ability to control dimming, obtaining ZVS for all power switches, decreased voltage stress on the switches, and enhanced efficiency. This paper is organized as section 2 gives description of proposed configuration. Section 3 presents the principle of operation and steady state analysis, sections 4 and 5 discuss design procedure and simulation results respectively. Finally, section 6 concludes the summary.

2. PROPOSED LED DRIVER

As the LEDs are equivalent DC loads, the block diagram of DC operated LED system is shown in Figure 1. LEDs give nonlinear output characteristics. The DC-DC converter in LED lighting system plays an important element to obtain uniform luminous output. The proposed full bridge-based LED configuration is illustrated in Figure 2. It drives three LED lamps, in which lamp-1 and 3 are identical, and lamp-2 power rating is different. All the three lamps are supplied through full bridge, which is configured with two legs. Leg-1 consists of two power MOSFETs, represented as (M_1&M_2), while leg-2 comprises of two power MOSFETs, designated as (M_3&M_4). D_1-D_4 and C_1-C_4 are body diodes and parasitic capacitances of M_1-M_4 respectively. Two different input voltages, V_{DC1} and V_{DC2} are arranged in an anti-series configuration, with their midpoint terminal denoted as '*O*'. Terminals *A* and *B* serve as the midpoints for leg-1 and leg-2, respectively. An inductor L_{ss} is connected between *A* and *B*, and current through L_{ss} is used for ZVS. v_{AB} is the output voltage of full bridge. In leg-1, the inductor $L_1$and LED lamp-1 are placed across switch M_1, while the inductor L_{i1} is connected in series with LED lamp-2 between terminal A and terminal O. In leg-2, inductor L_3 and LED lamp-3 are placed across switch M_3, while L_{i2} and LED lamp-2 are in series between B and O terminals. The high frequency current ripple in lamp-1 and lamp-3 are minimized by connecting series inductors L_1 and L_3, respectively. Current through lamp-2 is ripple free due to interleaved inductors L_{i1} and L_{i2}. A switch, S_{dim} is used for pulse-width modulation (PWM) dimming operation of all the lamps. V_{01}&i_{01}, V_{02}&i_{02}, and V_{03}&i_{03} are the output voltage and current in all three lamps respectively.

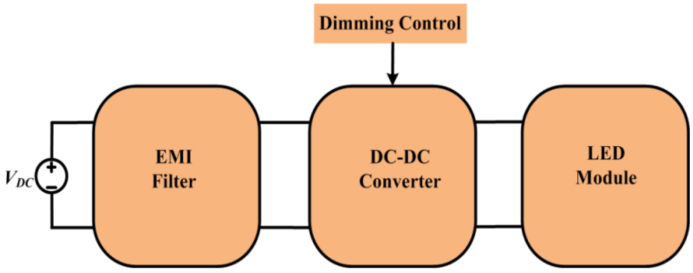


Figure 1. Block diagram DC operated LED system

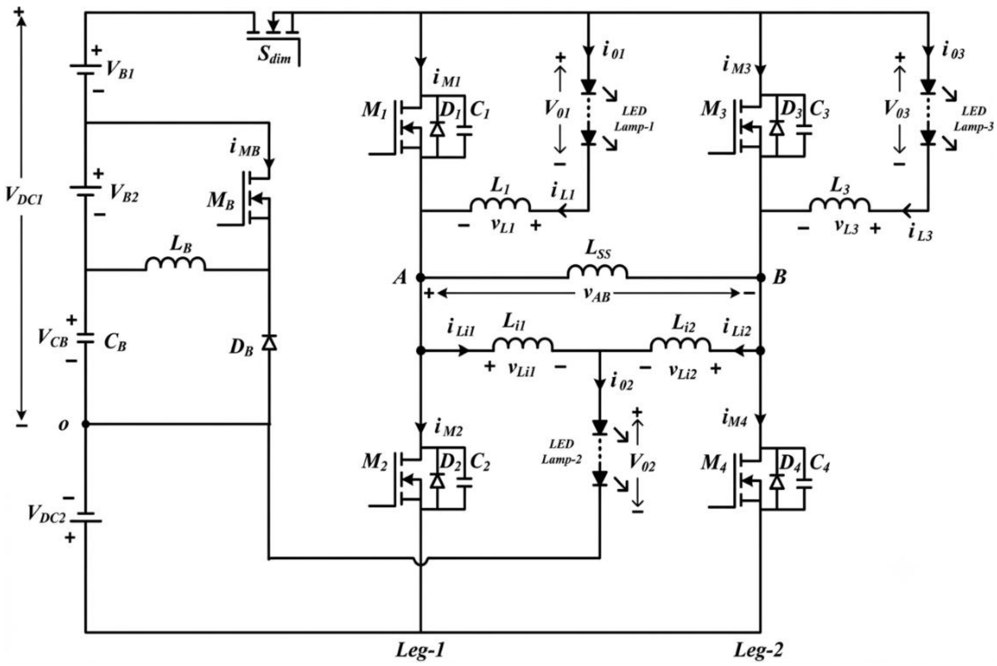


Figure 2. Circuit diagram of proposed LED driver

3. OPERATING MODES AND ANALYSIS

3.1. Converter operation

The operating waveforms are illustrated in Figure 3. Gate voltages of M_1 and M_4 are identical and represented as v_{g1} and v_{g4}. Similarly, gate voltages of M_2 and M_3 are also identical and represented as v_{g2} and v_{g3}. The converter operation in a switching frequency (f_s=1/T) is presented at equal duty ratio (D). This section explains the various modes of operation for the proposed LED driver.

a. Mode-1 (t_0–t_1)

At time t=t_0, gate voltages to devices M_1&M_4 are given and their conduction starts at zero drain to source (v_{M1}&v_{M4}) voltages. Figure 4(a) illustrates the corresponding equivalent circuit. From t_0–t_1, switches M_1&M_4 conduct and hence voltage (v_{AB}) across soft switching inductor, L_{ss} is+(V_{DC1}–V_{DC2}). Thus, current (i_{Lss}) in L_{ss} flows through M_1&M_4. In this mode, voltage across L_1 is–V_{01} and slope of i_{L1} is negative. In the same duration, voltage across L_3 is +(V_{DC1}–V_{DC2}–V_{03}) and slope of i_{L3} is positive.

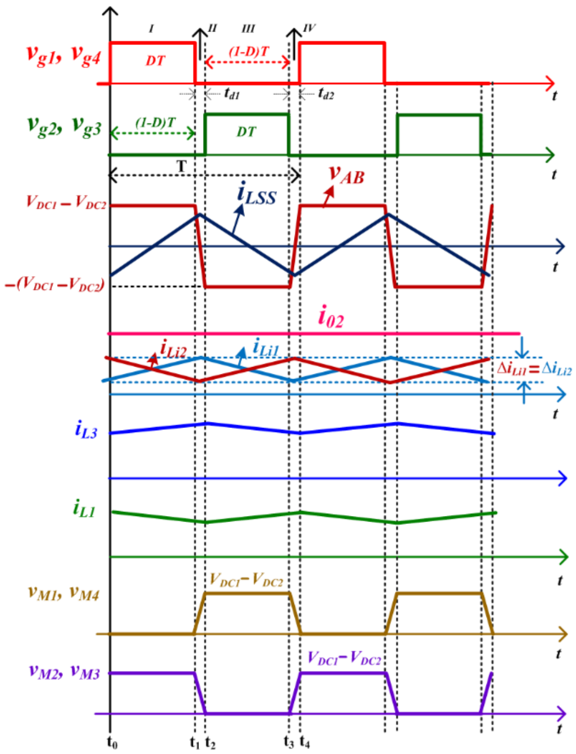


Figure 3. Operating waveforms

The current in interleaved inductor, L_{i1} increases linearly through M_1 due to the voltage (V_{DC1}–V_{02}) across it. At the same time, current in interleaved inductor, L_{i2} decreases linearly through M_4 due to the voltage (V_{DC2}–V_{02}) across it. Thus, current flowing through lamp-2 is the total of i_{Li1} and i_{Li2}. In this mode, switch M_1 conducts the sum of i_{Lss}, i_{L1}, and i_{Li1}. Similarly, M_4 conducts the sum of i_{Lss}, i_{L3}, and i_{Li2}. Hence, conduction losses in M_1&M_4 mainly depend on current in soft switching inductor (L_{ss}). Further, voltage across M_2&M_3 is (V_{DC1}–V_{DC2}). Hence switch off-state voltage is also reduced. This mode is stopped at $t=t_1$. The steady state mathematical expressions in this mode are given as (1) to (4):

$$v_{L1} + V_{01} = 0 \tag{1}$$

$$v_{Li1} - V_{DC1} + V_{02} = 0 \tag{2}$$

$$v_{L3} - V_{DC1} + (V_{DC2} + V_{03}) = 0 \tag{3}$$

$$v_{Li2} - V_{DC2} + V_{02} = 0 \tag{4}$$

The ripple current through L_1, L_{i1}, L_3, and L_{i2} are obtained as (5) to (8):

$$\Delta i_{L1} = i_{L1}(t_1) - i_{L1}(t_0) = \frac{-V_{01}}{L_1} DT \tag{5}$$

$$\Delta i_{Li1} = i_{Li1}(t_1) - i_{Li1}(t_0) = \frac{V_{DC1} - V_{02}}{L_{i1}} DT \tag{6}$$

$$\Delta i_{L3} = i_{L3}(t_1) - i_{L3}(t_0) = \frac{V_{DC1} - (V_{DC2} + V_{03})}{L_3} DT \tag{7}$$

$$\Delta i_{Li2} = i_{Li2}(t_1) - i_{Li2}(t_0) = \frac{V_{DC2} - V_{02}}{L_{i2}} DT \tag{8}$$

where $i_{L1}(t_0)$, $i_{Li1}(t_0)$, $i_{Li2}(t_0)$, and $i_{L3}(t_0)$ are starting inductor currents at $t=t_0$ for steady state operation. The difference between maximum and minimum current in L_1, L_{i1}, L_3, and L_{i2} are called as ripple current and written by using (5) to (8).

During t_1–t_0, the current in inductor, i_{Lss}, is expressed as (9):

$$i_{LSS}(t) = \frac{+(V_{DC1}-V_{DC2})}{L_{ss}}(t-t_0) + i_{LSS}\,(t_0)t_0 \le t < t_2 \tag{9}$$

b. Mode-2 (t_1–t_2)

At $t=t_1$ the gate voltages (v_{g1}&v_{g4}) are withdrawn and devices M_1 and M_4 stop conduction with zero-voltage (ZV) across them. The corresponding equivalent circuit is illustrated Figure 4(b). The switches M_2&M_3 are not yet started conduction and their parasitic capacitances C_2 and C_3 are charged to a voltage (V_{DC1}–V_{DC2}). From t_1–t₂ duration, parasitic capacitances C_1 is charged by current (i_{Lss}+i_{Li1}–i_{L1})/2 from zero to (V_{DC1}–V_{DC2}). At the same time, parasitic capacitances C_2 is discharged by (i_{Lss}+i_{Li1}–i_{L1})/2 from (V_{DC1}–V_{DC2}) to zero. Similarly, current (i_{Lss}+i_{L3}–i_{Li2})/2 discharges C_3, and (i_{Lss}+i_{L3}–i_{Li2})/2 charges C_4. When the voltage across C_2 and C_3 is –0.7 V, body diodes of M_2&M_3 start conducting. Thus, the gate voltages of M_2 and M_3 can be given for ZV(V_{M2}&V_{M3}) turn-on switching. This mode is stopped at $t=t_2$.

$$C_1 = C_2 = \frac{(i_{Lss}+i_{Li1}-i_{L1})}{2(V_{DC1}-V_{DC2})}(t_2-t_1) = \frac{(i_{Lss}+i_{Li1}-i_{L1})t_{d1}}{2(V_{DC1}-V_{DC2})} \tag{10}$$

$$C_3 = C_4 = \frac{(i_{Lss}+i_{L3}-i_{Li2})}{2(V_{DC1}-V_{DC2})}(t_2-t_1) = \frac{(i_{Lss}+i_{L3}-i_{Li2})t_{d1}}{2(V_{DC1}-V_{DC2})} \tag{11}$$

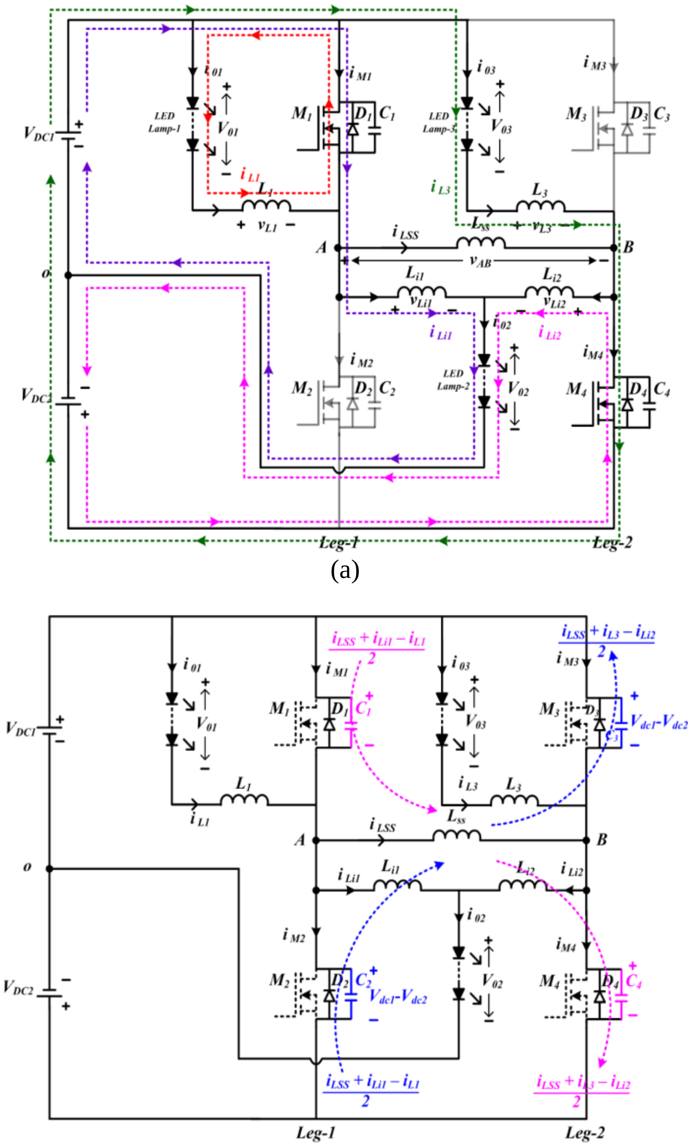


Figure 4. Operative circuits for; (a) mode-1 and (b) mode-2

c. Mode-3 (t_2–t_3)

At time $t=t_2$, gate voltages (v_{g2}&v_{g3}) to devices M_2&M_3 are given and their conduction starts at zero drain to source (v_{M2}&v_{M3}) voltages. Figures 5(a) and (b) illustrates corresponding equivalent circuit. From t_2–t_3, switches M_2&M_3 conduct, and hence voltage (v_{AB}) across soft switching inductor, L_{ss}, is–(V_{DC1}–V_{DC2}). Hence, current (i_{Lss}) in L_{ss} flows through M_2&M_3.

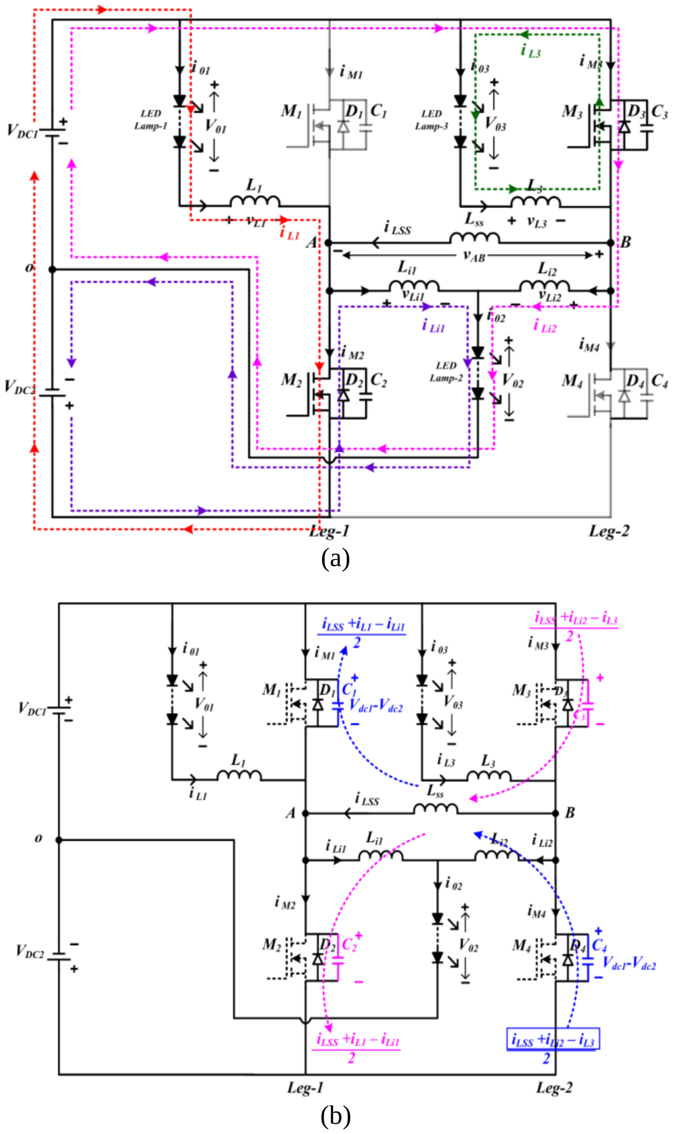


Figure 5. Operative circuits for; (a) mode-3 and (b) mode-4

In this mode, voltage across L_1 is (V_{DC1}–V_{DC2}–V_{01}). Hence, i_{L1} increases linearly through M_2. And, voltage across L_3 is–V_{03}. Hence, i_{L3} decreases linearly through M_3. The voltage across L_{i1} is (V_{DC2}–V_{02}) and L_{i2} is (V_{DC1}–V_{02}). Due to negative v_{Li1} and positive v_{Li2}, i_{Li1} decreases, and i_{Li2} increases linearly respectively. In this mode also, current flowing through lamp-2 is the total of i_{Li1} and i_{Li2}. Further, device M_2 conducts the sum of i_{Lss}, i_{L1}, and i_{Li1}. Device M_3 conducts the sum of i_{Lss}, i_{L3}, and i_{Li2}. Hence, conduction losses in M_2&M_3 mainly depend on current in soft switching inductor (L_{ss}). Further voltage across M_1&M_4 is (V_{DC1}–V_{DC2}). Hence, switch off-state voltage is also minimized. This mode is stopped at $t=t_3$. The steady state mathematical expressions are given as (12) to (15):

$$v_{L1} - V_{DC1} + V_{DC2} + V_{01} = 0 \quad (12)$$

$$v_{Li1} - V_{DC2} + V_{02} = 0 \quad (13)$$

$$v_{L3} + V_{03} = 0 \quad (14)$$

$$v_{Li2} - V_{DC1} + V_{02} = 0 \quad (15)$$

The ripple current through L_1, L_{i1}, L_3, and L_{i2} are obtained as (16) to (19):

$$\Delta i_{L1} = i_{L1}(t_3) - i_{L1}(t_2) = \frac{V_{DC1}-(V_{DC2}+V_{01})}{L_1}(1-D)T \quad (16)$$

$$\Delta i_{Li1} = i_{Li1}(t_3) - i_{Li1}(t_2) = \frac{V_{DC2}-V_{02}}{L_{i1}}(1-D)T \quad (17)$$

$$\Delta i_{L3} = i_{L3}(t_3) - i_{L3}(t_2) = \frac{-V_{03}}{L_3}(1-D)T \quad (18)$$

$$\Delta i_{Li2} = i_{Li2}\,(t_3) - i_{Li2}\,(t_2) = \frac{V_{DC1}-V_{02}}{L_{i2}}(1-D)T \quad (19)$$

Where $i_{L1}(t_2)$, $i_{Li1}(t_2)$, $i_{Li2}(t_2)$, and $i_{L3}(t_2)$ are the initial current values in L_1, L_{i1}, L_3, and L_{i2} from (t_2–t_3) duration respectively.
During t_3–t_2, current, $i_{Lss}(t)$, is expressed as (20):

$$i_{Lss}(t) = i_{Lss}(t_2) - \frac{(V_{DC1}-V_{DC2})}{L_{ss}}(t-t_2)t_2 \leq t < t_3 \quad (20)$$

d. Mode-4 (t_3–t_4)

During t_3 to t_4, switches (M_2&M_3) are switched off and switches (M_1&M_4) are switched on at ZV. This process is similar to that in mode-2. This mode ends at t=t_4 when charging and discharging of capacitances are completed.

$$C_1 = C_2 = \frac{(i_{Lss}+i_{L1}-i_{Li1})}{2(V_{DC1}-V_{DC2})}(t_3-t_2) = \frac{(i_{Lss}+i_{L1}-i_{Li1})t_{d2}}{2(V_{DC1}-V_{DC2})} \quad (21)$$

$$C_3 = C_4 = \frac{(i_{Lss}+i_{Li2}-i_{L3})}{2(V_{DC1}-V_{DC2})}(t_3-t_2) = \frac{(i_{Lss}+i_{Li2}-i_{L3})t_{d2}}{2(V_{DC1}-V_{DC2})} \quad (22)$$

3.2. Analysis

The switches in a full bridge configuration operate in steady state with equal durations for both ON and OFF states at a constant frequency. In the proposed converter, operating mode-1 and mode-3 are considered to derive V_{01}, V_{02}, and V_{03} expressions. When devices M_1 and M_4 conduct, stored energy in L_1dissipates in lamp-1, and lamp-3 is powered by V_{DC1}. Also, lamp-2 is fed from both V_{DC1} and stored energy in L_{i2}. When switches M_2 and M_3 are ON, lamp-1 is supplied by V_{DC1}, lamp-3 is powered by stored energy in L_3, and lamp-2 is fed from both V_{DC1} and stored energy in L_{i1}. In steady state operation, the duty ratio (D) of each MOSFET switch in the full bridge configuration is constant and uniform. From the principle of volt-sec balance, the output voltage V_{01}, V_{02}, and V_{03} are obtained as (23) to (25):

$$V_{01} = D(V_{DC1} - V_{DC2}) \quad (23)$$

$$V_{02} = D(V_{DC1} - V_{DC2}) + V_{DC2} \quad (24)$$

$$V_{03} = (1-D)(V_{DC1} - V_{DC2}) \quad (25)$$

4. DESIGN ASPECTS

In this study, LED lamp-1 and lamp-3 are identical. Equivalent electrical model [21] of LED is used to determine the values of various elements. From the voltage and current curve shown in Figure 6, it is identified that 2.3 V acts as the cut-in voltage (V_{Th}). For lamp-1 and lamp-3, an operating point (3 V, 340 mA) has been selected for each LED. In LED lamp-1 and lamp-3, there are three parallel strings, with each string consisting of four LEDs connected in series. Therefore, lamp-1 and lamp-3 are designed for 12 W. It is observed that output voltage (V_{01} (or) V_{03}) of lamp-1 (or lamp-2) is obtained as 12 V, and output current (i_{01} (or) i_{03}) through lamp-1 (or lamp-3) is 1.02 A.

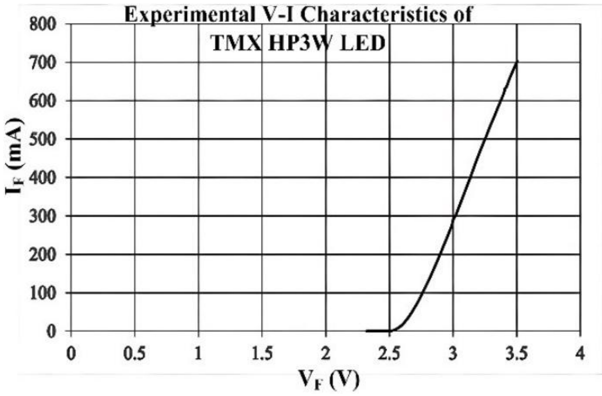


Figure 6. Forward characteristics of selected LED

An operating point (3.25 V, 510 mA) has been selected for LEDs in lamp-2. Lamp-2 employs two parallel strings, each consisting of 11 LEDs connected in series. Consequently, lamp-2 illuminates at 36 W. For lamp-2, 25.3 V acts as the total cut-in voltage. It has been noted that the output voltage (V_{02}) and current (i_{02}) in lamp-2 are calculated as 35.7 V and 1.02 A.
The input voltage across the full bridge is determined from (25).

$$V_{DC1} - V_{DC2} = \frac{12}{1-0.5} = 24V$$

In output voltage equation of V_{02}, V_{DC2} is not associated with D. The LED lamp does not operate below the cut-in voltage. Consequently, a voltage of 24 V is chosen for V_{DC2}, and $D(V_{DC1}–V_{DC2})$ is processed through full bridge converter. The input voltage V_{DC1} is expressed by using (24).

$$V_{DC1} - V_{DC2} = \frac{V_{02}-V_{DC2}}{D} \quad (26)$$

By substituting D=0.5, V_{DC2}=24 V, and V_{02}=35.75 V in (26).

$$V_{DC1} - 24 = \frac{35.75-24}{0.5} \Rightarrow V_{DC1} \cong 48\,V$$

Rearranging (16), value of L_1 is expressed as (27):

$$L_1 = L_3 = \frac{V_{DC1}-(V_{DC2}+V_{01})}{\Delta i_{L1}}(1-D)T \quad (27)$$

With D=0.5, V_{DC1}=48 V, V_{DC2}=24 V, V_{01}=12 V, and T=8 μs the inductor L_1 and L_3 values are calculated by using (27).

$$L_1 = L_3 = \frac{(48-(24+12))}{0.1\times1.02} \times (0.5) \times 8 \times 10^{-6} \cong 470\,\mu H$$

With D=0.5, V_{DC1}=48 V, V_{DC2}=24 V, V_{02}=13.75 V, and T=8 μs, the inductor L_{i1} and L_{i2} are calculated from (6).

$$L_{i1} = \frac{(48-35.75)}{0.408} \times (0.5) \times 8 \times 10^{-6} \cong 120\,\mu H = L_{i2}$$

To obtain ZV switching feature, it is required to produce an approximate constant current source for the charging and discharging of the output capacitors associated with the switches. An inductor L_{ss} is employed to produce the required constant current during dead time. The peak current flowing through L_{ss} is considered as a current source during the dead time. At $t=t_2$, the current i_{Lss} attains its maximum value, which is calculated by using (9).

$$i_{Lss-pk} = \frac{+(V_{DC1}-V_{DC2})DT}{2L_{ss}} \quad (28)$$

With a duty ratio of 0.5, the peak current through the L_{ss} is given (29):

$$i_{Lss-pk} = \frac{+(V_{DC1}-V_{DC2})T}{4L_{ss}} \quad (29)$$

The value of i_{Lss-pk} is inversely proportional to inductor L_{ss} for a fixed value of V_{DC1}, V_{DC2}, and T. With a L_{ss} of 40 µH, V_{DC1} of 48 V, V_{DC2} of 24 V, and a switching period T of 8 µs, the i_{Lss-pk}:

$$i_{Lss-pk} = \frac{+(48-24)8\times10^{-6}}{4\times40\times10^{-6}} = 1.2\ A$$

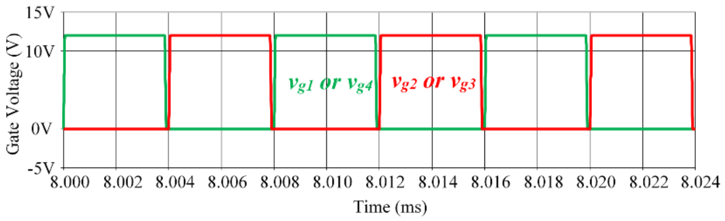
5. SIMULATION RESULTS

The proposed full bridge-based LED driver has been simulated in the OrCADPSpice environment with ideal inductors, capacitors, and DC input sources. However, IRF640N MOSFETs are used as switching devices. They have a voltage rating of 200 V, current rating of 18 A, on state resistance of 0.15 Ω, and maximum power dissipation of 150 W. The voltage, current, and power ratings of the LED lamp, along with the calculated component values, are given in Table 1. This configuration is simulated to supply a total output power of 60 W.

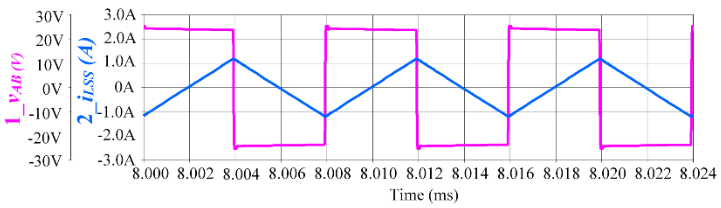
Table 1. Parameters of the proposed LED driver

Parameter	Value
DC input voltage, V_{DC1}	48 V
DC input voltage, V_{DC2}	24 V
Switching frequency, f_s	125 kHz
Soft-switching inductor, L_{ss}	40 µH
Inductor, $L_{1,3}$, L_3	470 µH
Inductor, L_{i1},L_{i2}	120 µH
Lamp-1 or lamp-3 voltage,V_{01},V_{03}	12 V
LED lamp-2 voltage,V_{02}	35.75 V
Current in lamp-1 and lamp-3,i_{01} (or) i_{03}	1.02 A
Current in lamp-2, i_{02}	1.02 A
P_{01}, P_{03}	12 W
P_{02}	36 W
Switching devices used	IRF640N

Figures 7(a) and (b) illustrates the gate voltages of the switches in the full bridge configuration, v_{AB} and i_{Lss} at rated power. It is observed that full bridge devices operate at D=0.5, $\pm$(48-24) is applied across L_{ss}. Figures 8(a)-(c) depicts the voltage and current waveforms for all lamps. The waveforms for both voltage and current are derived from selected values. It is observed that the voltage and current in lamp-1 and lamp-3 are identical. In contrast, lamp-2 exhibits V_{02} and i_{02} without any ripple, due to the use of interleaved inductors.

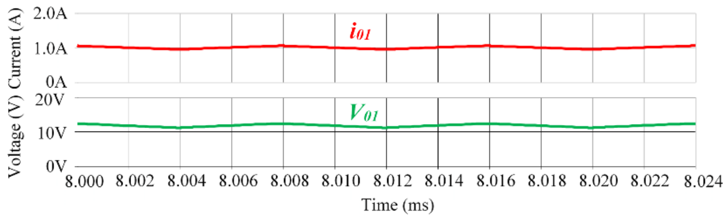


(a)

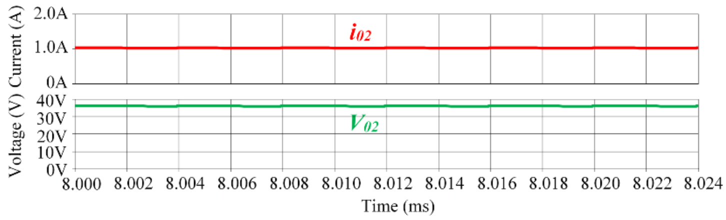


(b)

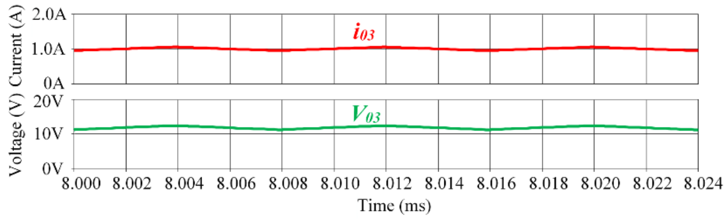
Figure 7. Simulation waveforms: (a) v_{g1}–v_{g4} and (b) v_{AB} and i_{Lss}



(a)



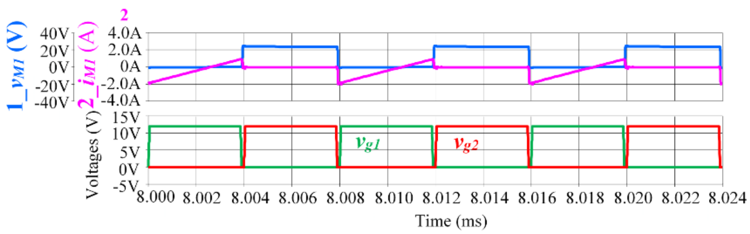
(b)



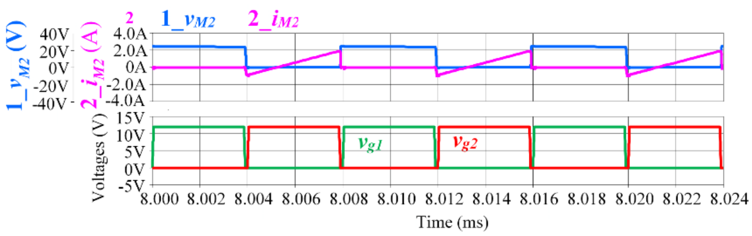
(c)

Figure 8. Voltage and current in all LED lamps:(a) LED lamp-1, (b) LED lamp-2, and (c) LED lamp-3

To show the ZVS characteristic in the proposed topology, Figures 9(a) and (b) illustrates the gate voltages, the voltage across, and the current through the switches in leg-1. The transitions of the devices in leg-1 from ON to OFF and from OFF to ON complete at ZV within the dead time. To integrate the dimming functionality of lamp currents, a switch S_{dim} is connected in series with V_{DC1}. This switch operates at a frequency of 100 Hz. It completely turns all the lamps ON and OFF at the selected operating current.



(a)



(b)

Figure 9. Switching waveforms for switches in leg-1: (a) gate voltages (v_{g1}–v_{g2}), voltage across, and current through M_1 and (b) gate voltages (v_{g1}–v_{g2}), voltage across, and current through M_2

Figure 10 illustrates the dimming waveforms for all the lamps. The lamp currents at 80%, 60%, and 40% dimming levels are represented in Figures 10(a)-(c) respectively. This clearly demonstrates that the lamps are operating at the selected current magnitudes, with their brightness regulated by a PWM dimming scheme.

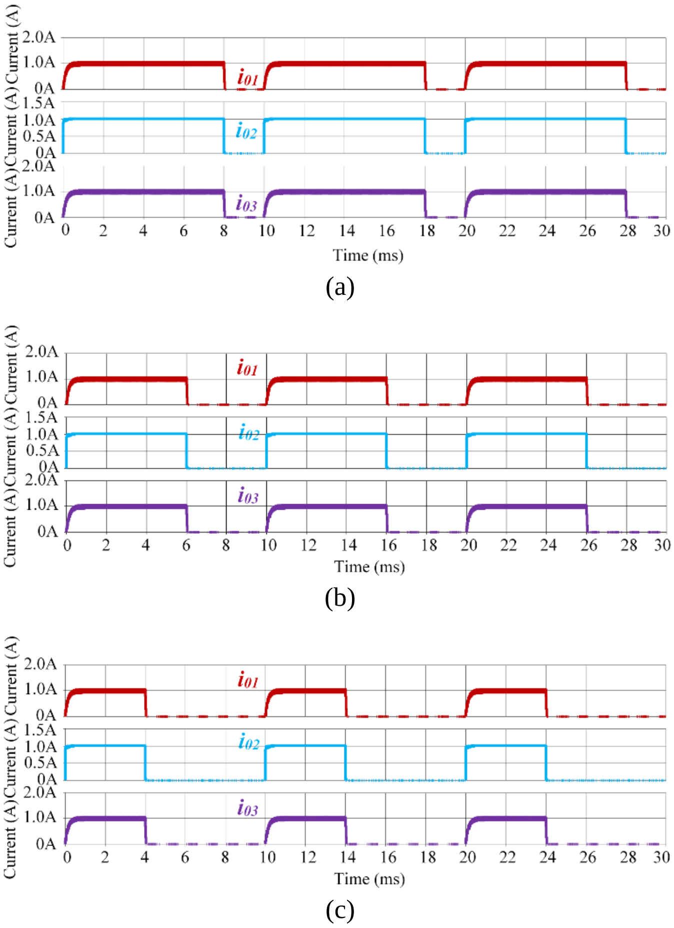


Figure 10. Dimming waveforms: (a) lamp currents at 80% dimming, (b) lamp currents at 60% dimming, and (c) lamp currents at 40% dimming

In the proposed configuration, regulation of lamp currents is verified at ±5% of input voltages. Figure 11 shows wave forms of gate voltage of M_B, current in L_B, and voltage across C_B at different input voltage levels. Figure 11(a) shows wave forms of gate voltage of M_B, current in L_B, and voltage across C_B at nominal input voltages, that is at V_{B1}=24 V, V_{B2}=12 V, and V_{DC2}=24 V. Figures 11(b) and (c) show the simulation waveforms at +5% and –5% variation in V_{B1}, V_{B2}, and V_{DC2}, respectively. It is observed that duty ratio of M_B is reduced at +5% increase in input voltages and it is reduced at –5% decrease in input voltages to maintain lamp operating point at selected values.

The key observations from simulation waveforms are presented as follows. The gate voltages, v_{g1}-v_{g4} are applied with 0.5 as duty ratio, 125 kHz as switching frequency and 100 ns as dead time. The full bridge output voltage v_{AB} is a square voltage with ±24 V magnitude, and the current i_{Lss} is a triangular waveform with ±1.19 A as peak value. A ripple current of 0.1016 A, 0 A, and 0.1017 A is observed in lamp-1, lamp-2, and lamp-3, respectively. The total power consumed by all three lamps is measured by using power dissipation marker as 61.249 W, and power supplied by DC sources is measured as 66.17 W. The total power loss in converter is obtained as 4.923 W. At full illumination, the proposed soft-switched LED driver achieves an efficiency of 92.56%.

Table 2 lists a comparative analysis of recent LED driver technologies as discussed in [21]-[25], along with the proposed converter for LED lighting applications. It particularly shows that the number of components per lamp in the proposed LED driver is lower than that of the LED drivers outlined in [21]-[25]. The efficiency at selected power is high and comparable with other topologies. The device voltage stress in proposed driver is less compared to the device voltage stress in topologies introduced in [21]-[25]. The performance of the proposed converter for LED lighting application has been validated using numerical simulation results. However, the converter validation using experimental results with closed loop operation will be extended as a future research work.

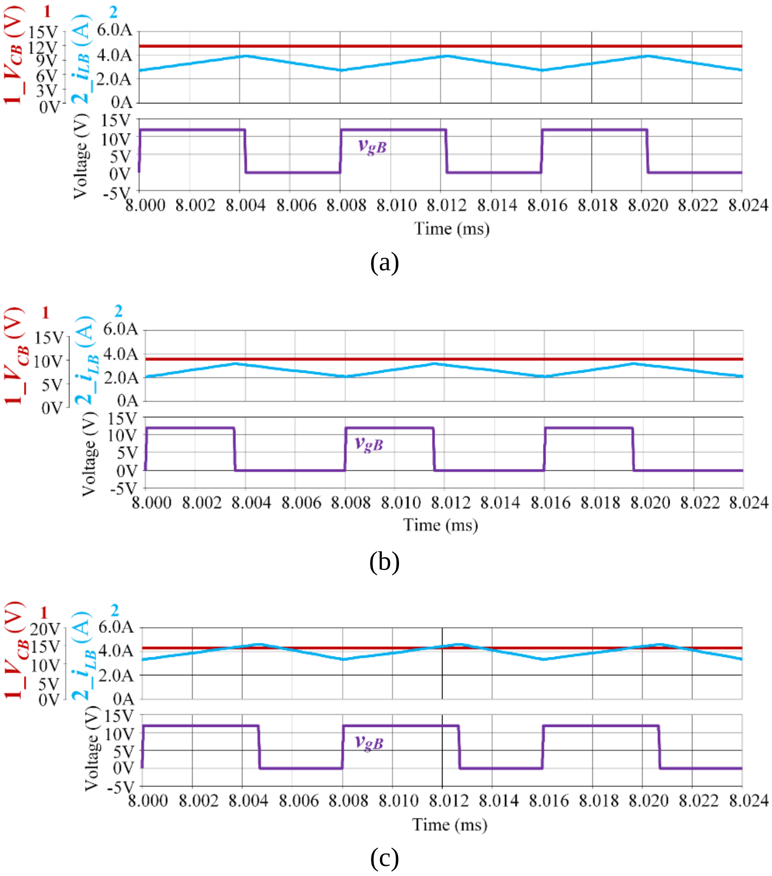


Figure 11. Waveforms of gate voltage of M_B, current in L_B, and voltage across C_B at different voltage levels at; (a) nominal, (b) +5%, and (c) -5% in input voltages

Table 2. Comparative analysis with recent similar LED driver technologies

Parameter		[21]	[22]	[23]	[24]	[25]	Proposed
Number of components	S	6	3	5	6	6	6
	L	3	2	3	4	4	6
	D	8	6	8	0	0	1
	C	4	6	5	2	2	1
	T/F	0	0	0	0	0	0
Input voltage		48 V	48 V	48 V	24 V	24 V	48 V
Output power		126 W	50 W	65 W	80 W	80 W	60 W
Number of LED lamps		2	2	2	2	2	3
Components count per lamp		10.5	9.5	10.5	6	6	3.5
Peak efficiency		92.45%	91%	92.3%	94.24%	94.24%	92.56%
Device stress		V_{dc}	V_{dc}	$2V_{dc}$	V_{dc}	V_{dc}	$<V_{DC}$

Note: S: switch; L: inductor; D: diode; C: capacitor; and T/F: Transformer.

6. CONCLUSION

This research paper introduces a novel full bridge LED driver configuration that utilizes two input voltages to power various LED lighting loads. The suggested driver topology is designed to reduce voltage stress while ensuring high energy efficiency. A thorough analysis of steady-state behavior is included to offer a detailed understanding of the circuit's operation. To confirm the proposed design, extensive simulation results are presented. The primary characteristics that include ZVS operation, ability to power multiple lighting loads, dimming operation, and regulation of lamp current via input voltage control. Additionally, a comparison with recent topologies in the literature underscores the benefits of the proposed design. This driver is particularly suitable for applications involving multiple loads and can be powered by both solar and battery sources, rendering it a practical solution for modern, energy-efficient lighting systems. However, the scalability of the proposed design is limited in high power multi-load lighting applications.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing -**O**riginal Draft
E : Writing - Review &**E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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