

Finite-set MPC for a 7-level cascaded H-bridge simulation-based evaluation with reference extrapolation and non-idealities

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ABSTRACT

Multilevel cascaded H-bridge (CHB) inverters are widely used in power conversion systems because they can create high-quality voltage waveforms with low harmonic distortion. However, the predictive control of multilevel converters faces challenges such as computational delays, switching dynamics, and maintaining performance under nonideal conditions. This study explores finite-control-set model predictive control for a three-phase seven-level CHB inverter with an inductor capacitor inductor (LCL) filter, taking into account hardware-related imperfections. A discrete state-space model and a voltage-tracking cost function are used to assess 343 possible switching vectors at each sampling interval. Second-order reference extrapolation is applied to manage the typical one-sample actuation delay in real-time digital systems. Simulation results show that, in ideal conditions, the inverter achieves a voltage total harmonic distortion (THD) of less than 0.1% and a power factor close to one. Under realistic disturbances, such as dc-link voltage drops and load imbalances, the system remained stable, with the THD increasing slightly to approximately 5%. Thus, the controller maintains good waveform quality and dynamic stability despite common disturbances in converter operations and digital control limits. The main contribution is integrating second-order reference extrapolation within a hardware-aware finite-control-set model predictive control (FCS-MPC) framework, providing a practical basis for future real-time implementation and validation through processor-in-the-loop (PIL) or hardware-in-the-loop testing.

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1. INTRODUCTION

Multilevel cascaded H-bridge (CHB) inverters have attracted significant attention due to their ability to synthesize high-quality voltage waveforms with reduced harmonic distortion and lower switching stress. Sharma [1] investigated harmonic optimization in CHB inverters and highlighted the trade-off between harmonic performance and circuit complexity. Ahamad *et al.* [2] analyzed the performance of solar-driven CHB multilevel inverters and demonstrated improved output voltage quality in renewable energy systems. Ahmad *et al.* [3] studied the application of multilevel inverters in grid-connected photovoltaic systems and emphasized their capability to enhance power quality. Meanwhile, Farooq *et al.* [4] proposed a high-power multilevel inverter topology designed to achieve low harmonic distortion in large-scale power applications. These studies confirm the effectiveness of CHB-based multilevel inverters for high-quality power conversion.

In a three-phase 7-level CHB configuration with an inductor capacitor inductor (LCL) filter, however, several practical challenges remain prominent: maintaining power quality total harmonic distortion (THD) [5]-[7], controlling switching behavior under a quantized action set, and preserving robustness in the presence of component non-idealities and controller latency during real-time deployment [8]-[10]. On the control side, finite-control-set model predictive control (FCS-MPC) has emerged as a promising control strategy for power electronic converters because it directly selects switching states without requiring modulation stages and can explicitly handle system constraints. Predictive control has been widely investigated in power electronics due to its fast dynamic response and flexibility in multi-variable control problems [11], [12]. Ramírez *et al.* [13] applied FCS-MPC to a CHB inverter and demonstrated improved current control performance. Easley *et al.* [14] proposed a hierarchical MPC framework to improve control performance in grid-connected cascaded multilevel inverters. More recently, Zafra *et al.* [15] explored long prediction horizon strategies to enhance predictive control performance in power electronic converters. Despite these advances, several practical challenges remain, particularly related to switching behavior, computational delay, and robustness under non-ideal operating conditions. For a three-phase seven-level CHB inverter, each phase can realize $\{-V_{dc}, 0, +V_{dc}\}$ at the cell level, yielding seven phase levels $(-3 \dots +3)$ and a reduced 343-vector action set per sampling step [16]. A discrete state-space model and stage cost are evaluated for all candidates, and the switching vector with the lowest cost is applied. In practice, classical FCS-MPC may exhibit a non-constant switching frequency [17], sensitivity to plant parameters [18], and computational delay [19], [20] as well as degraded power quality when realistic non-idealities are taken into account.

Recent research has investigated predictive control strategies for power electronic systems, including improved switching optimization, long-prediction-horizon formulations, and real-time implementation techniques. Comprehensive reviews of MPC for power electronics highlight its advantages in handling nonlinear dynamics and switching constraints while also identifying challenges related to computational complexity and implementation delays [21].

Despite significant progress in predictive control of multilevel inverters, several practical aspects remain underexplored, particularly for CHB systems operating under realistic implementation conditions. First, the influence of reduced switching vector sets on harmonic performance in high-level CHB inverters has not been thoroughly analyzed, even though switching-state quantization may limit achievable power quality [22]. Second, many predictive control studies assume ideal computation and actuation timing, while real digital controllers inevitably introduce sampling delays that can affect tracking accuracy and stability; therefore, practical and computationally efficient delay compensation methods remain an important research topic [23]. Third, the robustness of predictive control under practical disturbances such as dc-link voltage variations and phase load imbalance, which may introduce negative- and zero-sequence components in three-phase systems, has not been extensively investigated [24]-[26]. Addressing these issues is essential for bridging the gap between simulation-based predictive control studies and their practical deployment in processor- or HIL platforms and real embedded systems [27].

Despite notable advancements in the predictive control of multilevel inverters, several practical considerations remain insufficiently explored, particularly concerning CHB systems operating under realistic implementation conditions. Firstly, the impact of reduced switching vector sets on harmonic performance in high-level CHB inverters has not been comprehensively analyzed, even though switching-state quantization may constrain achievable power quality. Secondly, numerous predictive control studies presuppose ideal computation and actuation timing, whereas real digital controllers inevitably introduce sampling delays that can affect tracking accuracy and stability. Consequently, the development of practical and computationally efficient delay compensation methods remains a significant research area. Thirdly, the robustness of predictive control under practical disturbances, such as dc-link voltage variations and phase load imbalance, has not been extensively investigated. Addressing these issues is crucial to bridging the gap between simulation-based studies and real-time implementation.

This study contributes: i) a compact FCS-MPC formulation for a three-phase 7-level CHB with second-order reference extrapolation to compensate for a one-sample actuation/compute delay while keeping the algorithm lightweight; ii) a hardware-aware evaluation that incorporates driver dead-time, sensor quantization/noise, passive losses, and outside disturbances (dc-link sag and load unbalance); and iii) a robustness analysis explained through switching cost (SWC) heatmaps and harmonic spectra, together with actionable tuning guidelines—light current-error weighting and a modest switching penalty. All analyses were conducted within a single, consistent abc state-space frame to avoid modeling–execution mismatch.

The study strictly follows the provided simulink model (SLX) and MATLAB control functions used in the implementation. The controller performs one-step prediction and candidate selection with a voltage-centric tracking cost (as implemented), while introducing nonidealities in the plant and measurement paths to ensure that the core algorithm remains the same. This setup yields results that are both representative of real hardware behavior and reproducible by researchers and practitioners using the same model files.

Paper organization. Section 2 presents the converter model, FCS–MPC scheme, second-order reference extrapolation, and placement/parameters of non-idealities. Section 3 reports the simulation results for the baseline, delay-compensated, and disturbed (dc-link sag+unbalance) scenarios, discusses the implications, limitations, and tuning guidelines for processor-in-the-loop (PIL)/HIL. Section 4 concludes the paper.

2. METHOD

2.1. Topology and discrete model

We consider a three-phase 7-level CHB inverter supplying a three-phase load through an LCL filter (L1, Cf, and L2), as shown in Figure 1. The study operates in a stand-alone mode; the grid voltage is retained in the model for completeness but set to zero in all simulations ($v_g=0$). A fixed sampling time of $T_s=25\ \mu\text{s}$ was used with zero-order hold discretization, yielding a linear time-invariant discrete-time plant.

$$x_{k+1} = \Phi x_k + \Gamma u_k + \tau v_g, k \quad (1)$$

Where $x \in \mathbb{R}^9$ stacks the phase currents and capacitor voltages:

$$x = [i_{L1,a}, i_{L1,b}, i_{L1,c}, i_{L2,a}, i_{L2,b}, i_{L2,c}, v_{C,a}, v_{C,b}, v_{C,c}]^T$$

where $u_k = [V_{inv,a}, V_{inv,b}, V_{inv,c}]^T$, is the inverter phase voltage vector at the filter input. For each phase, $v_{inv,\phi}$ the results from the series sum of three H-bridge cells with switching states $\{-V_{dc}, 0, +V_{dc}\}$, produce seven available levels $\{-3, -2, -1, 0, +1, +2, +3\}$ Vdc per phase. In all stand-alone cases, $v_{g,k}=0$. The measured feedback signals are $i_{L1,\phi}$, $i_{L2,\phi}$, and $v_{C,\phi}$ for, $\phi \in \{a, b, c\}$ which directly map to the state vector above.

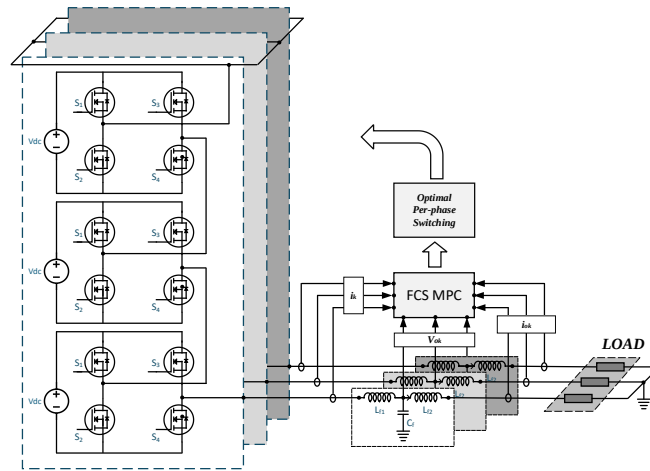


Figure 1. CHB 7-level circuit topology with LCL filter

2.2. Finite-set model predictive control

At each sampling step k , the controller evaluated 343 candidates (seven phase levels per phase, three phases). For the i -th candidate $u_k^{(i)}$, one-step prediction as (2):

$$x_{k+1}^{(i)} = \Phi x_k + \Gamma u_k^{(i)} + \tau v_{g,k} \quad (2)$$

where $v_{g,k}=0$ for stand-alone. In each sample, 343 candidates were evaluated, and the minimum-cost candidates were mapped to 18 gate signals (2 per cell $\times$ 3 cells/phase). The procedure for each sample is summarized in Figure 2. The prediction components used for the evaluation were $\hat{i}_0^{k+1}(i)$ and $\hat{v}_0^{k+1}(i)$. Candidates with minimum cost are mapped to the 18 gate drive signals (2 per cell $\times$ 3 cells/phase).

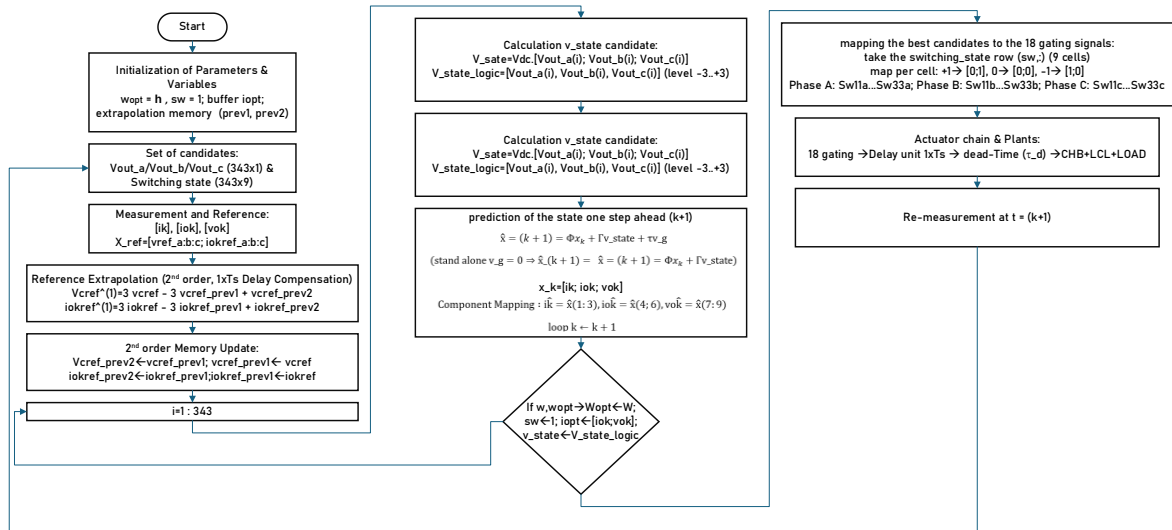


Figure 2. Per-sample FCS-MPC flow

2.3. Reference extrapolation

Because the decision at step k is applied at $k+1$, we project the references one step ahead using second-order extrapolation as (3) and (4):

$$\tilde{v}_{c,ref}[k+1] = 3v_{c,ref}[k] - 3v_{c,ref}[k-1] + v_{c,ref}[k-2] \quad (3)$$

$$\tilde{i}_{L2,ref}[k+1] = 3i_{L2,ref}[k] - 3i_{L2,ref}[k-1] + i_{L2,ref}[k-2] \quad (4)$$

These forward-projected references are used in the stage costs.

2.4. Cost function and candidate selection

In accordance with the design focus (voltage tracking at node C_f), the costs used are voltage-based as (5):

$$J(i) = \sum_{\phi \in \{a,b,c\}} |\tilde{v}_{c,ref\phi}[k+1] - v_{c,\phi}^{(i)}[k+1]|^2 \quad (5)$$

Selected $i^* = \arg \min_i J(i)$; candidate switch pattern i^* is generated for all three phases; then, the associated switch pattern is applied through the candidate map in the available H-bridge cell in the model. We denote the stage cost by J ; in the MATLAB/Simulink implementation, the same scalar is stored in variable w .

2.5. Hardware-aware non-idealities

To keep the simulations representative of the hardware while leaving the control algorithm unchanged, we inject the following non-idealities in the plant and measurement paths:

- Actuation/compute delay: a one-sample delay T_s on all 18 gate signals, such that the decision taken at step k is applied at $k+1$.
- Driver dead time: a symmetric non-overlapping interval $\tau_d=2 \mu s$ per leg (no explicit dead-time compensation).
- Disturbance scenarios (stand-alone); i) dc-link droop to 0.7 pu and ii) 20% phase-to-phase load unbalance implemented by perturbing the per-phase R/L. All other parameters were maintained at their nominal values across the cases.
- THD estimation: the THD is computed from steady-state windows spanning an integer number of fundamental cycles (≥ 5) after the initial synchronization transient. We enforced coherent sampling (no window) and aligned the FFT bins at 50 Hz to suppress spectral leakage.

2.6. Implementation MATLAB/Simulink

In (1)–(5) were implemented in MATLAB/Simulink (fixed-step discrete solver, $T_s=25 \mu s$). The controller is implemented as a MATLAB function that evaluates 343 candidates at each step, predicts $\hat{x}_{k+1} =$

$\Phi x_k + \Gamma v_{\text{state}}^{(i)}$ (stand-alone mode, $v_g=0$), applies 2nd-order reference extrapolation to $v_{(c,\text{ref})}$ and $i_{(o,\text{ref})}$, and then selects the candidate with the minimum cost (5). The control output consists of 18 gate signals that pass through a $1 \times T_s$ delay unit and dead time before the power leg. Sensor non-idealities are modeled in the feedback path (noise + quantizer with steps ΔI , ΔI_O , and ΔV). The controller input port sequence is arranged as Port-1= i_{ok} , Port-2= v_{ok} , Port-3= x_{ref} , and Port-4= i_k (each a 3×1 column vector). A list of V_{out} candidates and a map of the 18 gate signals are provided in the workspace. The slx and m files are provided in the supplementary material.

3. RESULTS AND DISCUSSION

All simulations were executed in MATLAB/Simulink with a fixed-step discrete solver at $T_s=25 \mu\text{s}$. The controller evaluated 343 candidates per step in a MATLAB Function block, and profiling confirmed an ample timing margin relative to the sampling budget. The working parameters of this simulation are listed in Table 1.

Table 1. Simulation operating parameters

No	Parameter	Symbol	Value	Units
1	Source voltage	Vdc	133	V
2	Voltage source capacitor	Cdc	2.350×10^{-6}	F
3	Voltage source resistance	Rdc	1×10^{-3}	Ω
4	Sampling time	T_s	25×10^{-6}	s
5	First inductor in LCL filter	L1	10×10^{-3}	H
6	Second inductor in LCL filter	L2	0.6×10^{-3}	H
7	Capacitor in LCL filter	C_f	20×10^{-6}	F
8	Resistance in LCL filter	R1, R2	0.1	Ω
8	Load	P	1000	Watt
9	Operating frequency	f	50	Hertz

3.1. Baseline performance

Under ideal conditions (no actuation delay, no dead time, ideal sensors, and lossless LCL), the capacitor node voltage v_{ok} closely tracks its sinusoidal reference, and the load current i_{ok} is nearly in phase for a resistive load (power factor (PF) ≈ 0.99). The phase-average THD is very low (e.g., $\text{THD}_v \approx 0.01\%$), which is consistent with the seven-level synthesis.

Figure 3 illustrates the steady-state waveforms of the capacitor voltage (v_{ok}) and output current (i_{ok}). It can be observed that the voltage waveform closely follows the sinusoidal reference with minimal distortion, whereas the current remains nearly in phase, confirming high-power-factor operation. This demonstrates the effectiveness of the voltage-tracking FCS-MPC strategy under ideal conditions.

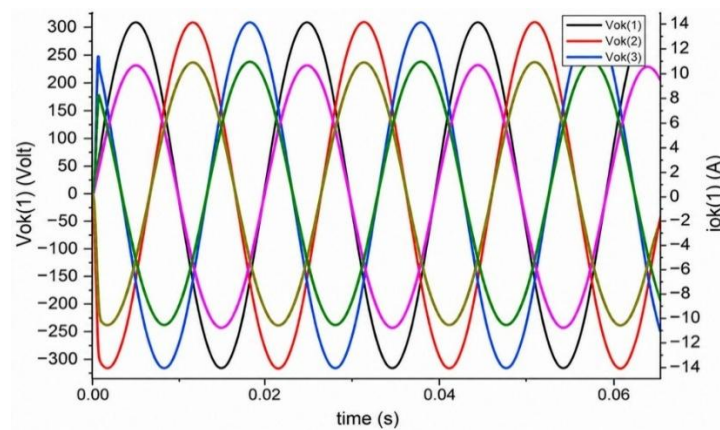


Figure 3. Waveform v_{ok} and i_{ok} shown $\text{PF} \approx 0.99$

Figures 4(a) and (b) shows the harmonic spectrum of the voltage and current signals. The extremely low THD values ($\approx 0.01\%$) indicate that the seven-level CHB inverter combined with predictive switching selection can significantly suppress the harmonic components. This validates the capability of the proposed method to achieve high-quality voltage synthesis. The test parameters are listed in Table 2.

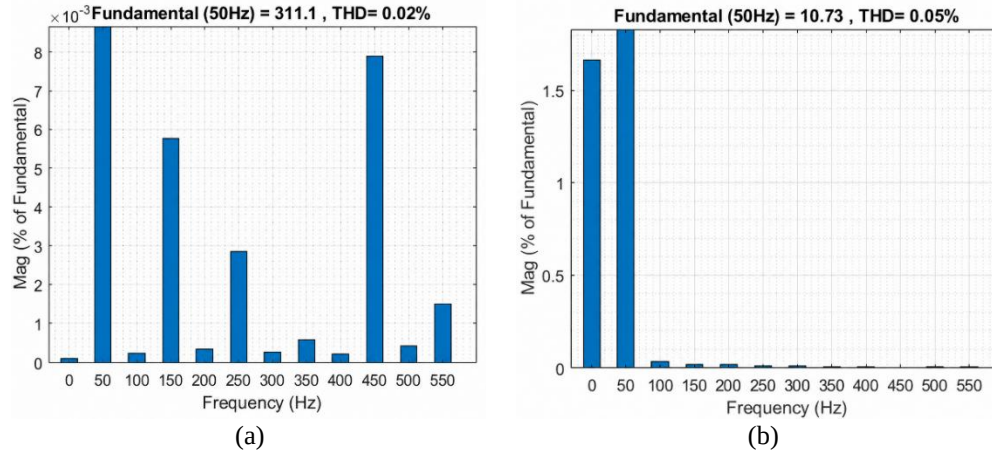


Figure 4. Harmonic spectrum and THD of phases a, b, and c; (a) voltage and (b) current

Table 2. Simulation result parameter

No	Parameter	Phase	Value	Unit
1	THDVok	a	0.01	%
		b	0.01	%
		c	0.01	%
2	THDiok	a	0.12	%
		b	0.05	%
		c	0.08	%
3	PF	-	≈0.99	
4	VRMSE	a	0.03	
		b	0.03	
		c	0.03	

Figure 5 shows the SWC heatmap under the conditions $T_s=25 \mu s$, $f_s=40 \text{ kHz}$, and $f_0=50 \text{ Hz}$. The heatmap exhibits a consistently repeating horizontal band pattern, indicating a stable and periodic candidate selection mechanism in the FCS-MPC controller for the three-phase 7-level CHB inverter with an LCL filter ($L_1=10 \text{ mH}$, $L_2=0.6 \text{ mH}$, $C_f=20 \mu F$, $R_1=R_2=0.1 \Omega$, and $V_{dc}=133 \text{ V}$).

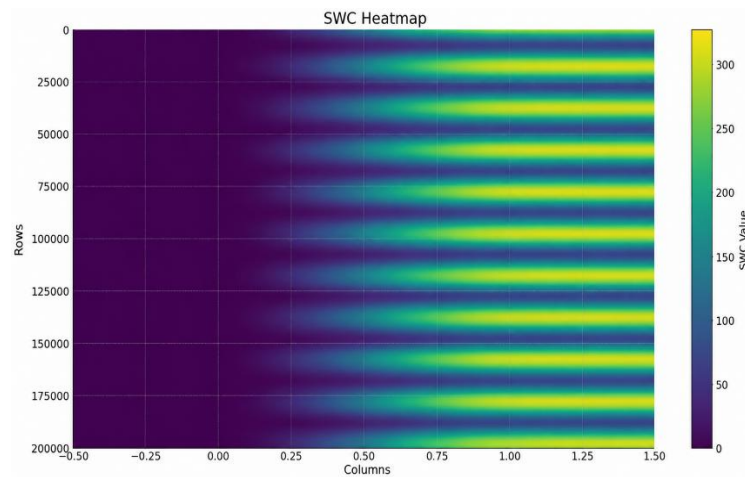


Figure 5. Heatmap SWC

With an action space consisting of 343 possible switching combinations and a voltage-centric cost function $w = \sum_{a,b,c} |\hat{v}_c - \hat{v}_{c,ref}|^2$ based on one-step extrapolated references, the optimal switching indices are concentrated in several adjacent “bands.” This behavior indicates that the controller consistently selects voltage levels close to the reference, thereby enabling accurate capacitor voltage tracking with moderate switching activity.

Furthermore, the clustering of switching selections around the zero-crossing region suggests the absence of an explicit switching penalty in the cost function, which leads to an increased switching density in this region. This observation provides important insights into the trade-off between tracking accuracy and switching losses and highlights a potential direction for future improvement by introducing a small switching penalty or current-weighting term. Overall, the SWC heatmap confirmed stable operation, consistent decision patterns, and effective voltage-tracking performance under the tested conditions.

3.2. Delay $1 \times T_s$ + reference extrapolation impact

Two cases are compared: a one-sample actuation delay without extrapolation and with second-order reference extrapolation, as shown in Figures 6(a) and (b). A one-sample delay introduces a small phase bias between the reference and actual voltage waveforms; however, the overall waveform shape remains visually close to the baseline case.

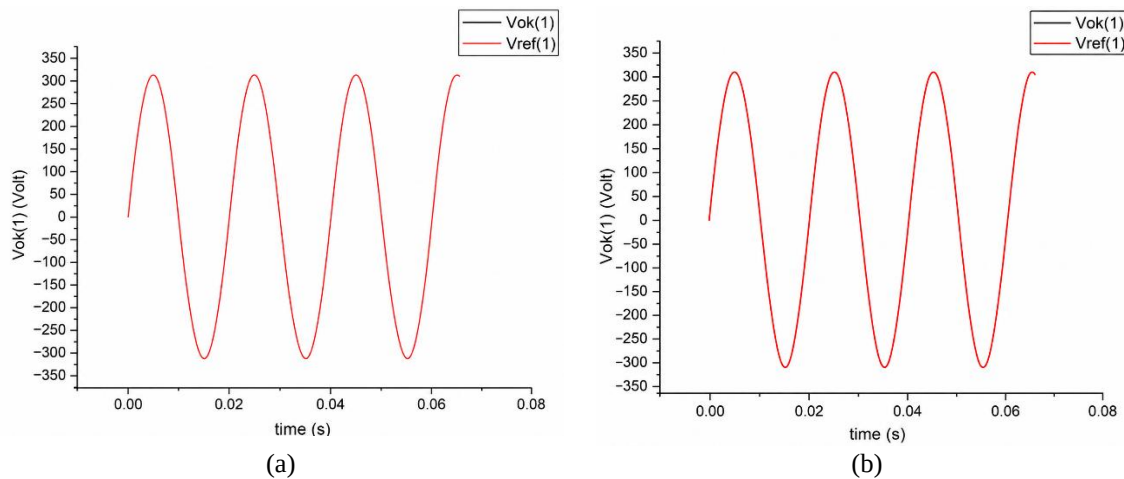


Figure 6. Comparison Vok and Vref; (a) baseline and (b) $1 \times T_s$ 2nd-order extrapolation

When the second-order reference extrapolation is enabled, this residual phase shift is eliminated, improving the alignment between the reference and measured voltages. This demonstrates that the proposed extrapolation method can compensate for digital control delay without altering the fundamental waveform characteristics. As a result, the extrapolation serves as an effective hardware-aware compensation strategy for practical implementations.

Figure 7 provides a quantitative comparison of the phase-average voltage THD for the baseline and delayed cases. Without reference extrapolation, THDv increased modestly from 0.01% to 0.05% (+0.04%), confirming the presence of delay-induced distortion. When second-order extrapolation was applied, the THD values returned close to the baseline, with only marginal variations ($\Delta\text{THD} \approx 0-0.04\%$ across phases).

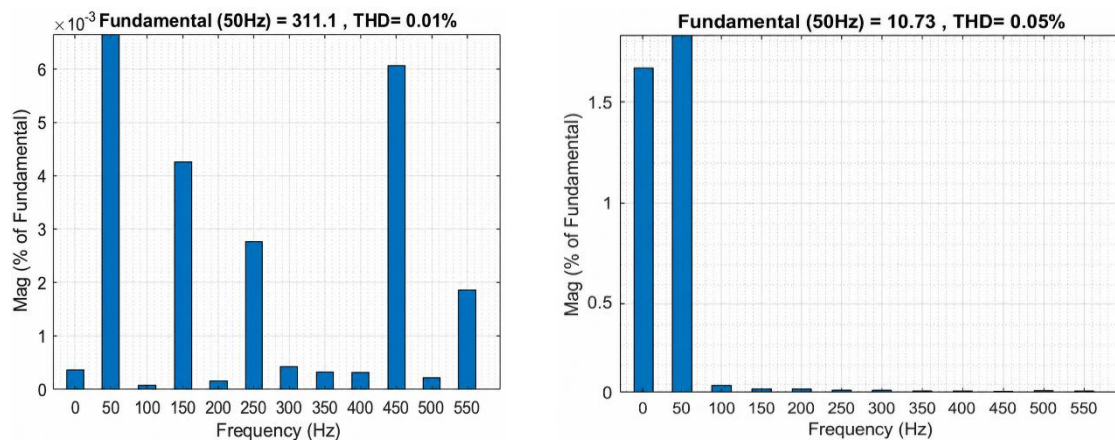


Figure 7. Comparison of THD Vok baseline and Vok with delay and 2nd-order extrapolation

In addition, the corresponding RMS variations remain small ($\Delta\text{RMS}\approx 0.5\text{--}1\%$), indicating that the delay has a negligible impact on the overall power quality when properly compensated. These results confirm that the second-order reference extrapolation effectively mitigates the effect of actuation delay while preserving both the waveform quality and system stability. The numerical results are summarized in Table 3.

Table 3. Delay and extrapolation on THD, RMSE, and PF

Parameter	Phase	Value	Unit
THDVok	a	0.01	%
	b	0.01	%
	c	0.01	%
THDiok	a	0.12	%
	b	0.05	%
	c	0.07	%
PF	-	≈ 0.99	
VRMSE	a	0.03	
	b	0.03	
	c	0.03	

3.3. Dead-time impact

With $\tau_d \approx 2\ \mu\text{s}$, dead time causes a minor amplitude reduction near zero crossings and a negligible effect on the phase-average THD and PF for the tested resistive loading. We report this as a marginal non-ideality and omit the detailed tables for brevity.

Empirical data demonstrate that increasing the resolution of the analog-to-digital converter (ADC) results in a quantifiable reduction in the quantization noise floor. This observation is consistent with theoretical predictions, as an increased bit depth offers a more precise discretization of the signal, consequently diminishing the variance of the quantization error and slightly enhancing the root mean square error of the voltage (VRMSE).

However, it was discovered that the effect on THD was minimal. For the designated reporting window, the recorded variations in THD across various resolution settings remained within the measurement uncertainty margin and environmental noise floor. We provided a qualitative synthesis of the ADC-induced noise effects because these variations were not statistically significant and did not change the main conclusions of the study. To keep the manuscript brief and prioritize the discussion of the main performance drivers, detailed numerical tables for these parameters have been omitted.

3.4. Robustness (Vdc droop and unbalance)

3.4.1. Direct current link droop

Robustness was tested by; i) dropping Vdc to 0.7 pu in a separate test and ii) applying a 20% interphase load unbalance. The controller maintained voltage tracking with a short settling time and without excessive oscillation, and the current remained stable even though the amplitude was adjusted. After the disturbance, the THD and PF returned to near pre-disturbance conditions. A small zero-crossing skew of approximately 0.27–0.32 ms ($\approx 1.5\%$ of a 50-Hz cycle, $\sim 5\text{--}6^\circ$) is observable without extrapolation and is effectively removed when the second-order extrapolation is enabled.

3.4.2. Unbalanced load

Testing under unbalanced conditions was performed by introducing a 20% phase-to-phase load-imbalance. The resulting voltage and current waveforms are presented in Figure 8. Despite the disturbance, the controller maintained stable operation and accurate voltage tracking. The waveforms remained well-regulated, although a slight asymmetry appeared owing to the load imbalance. The THD increased to approximately 5% across all phases, whereas the PF remained close to unity ($\text{PF}\approx 0.99$), indicating robust performance under nonideal conditions.

To further analyze the harmonic behavior under these conditions, the corresponding voltage and current spectra are shown in Figures 9(a) and (b). The spectra clearly show the dominant low-order harmonics, particularly the 3rd, 5th, and 7th components, which become more pronounced owing to the combined effect of load imbalance and switching-state quantization.

Compared to the ideal case ($\text{THD}_v\approx 0.01\%$, $\text{VRMSE}\approx 0.03\ \text{pu}$, and $\text{PF}\approx 0.99$), the increase in THD under the disturbed conditions reflects the inherent limitation of the discrete switching levels and their interaction with the LCL filter dynamics. Additionally, the denser switching-state clustering near the zero-crossing regions, observed in the SWC heatmap, is consistent with the use of a voltage-centric cost function without an explicit switching penalty.

Furthermore, when the dc-link voltage droop (0.7 pu) was combined with a load imbalance, the controller continued to maintain stability and acceptable waveform quality. Although the THD increased to approximately 5%, the system remained well controlled, and no instability or excessive oscillation was observed. These results confirm that the proposed control strategy is robust against practical disturbances while maintaining an acceptable power quality.

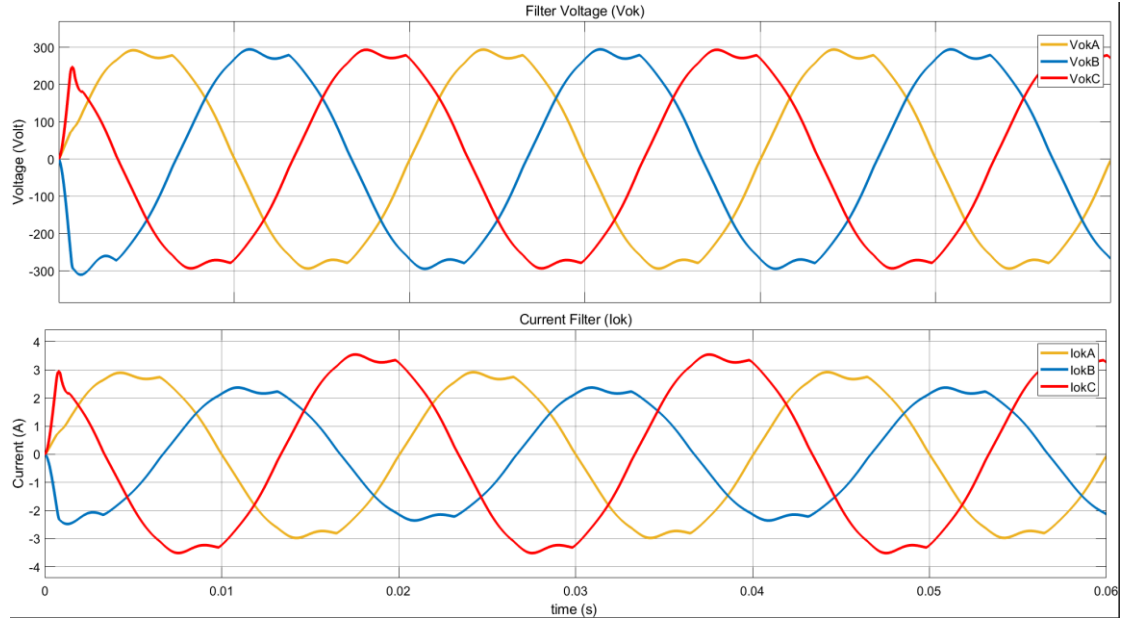


Figure 8. Waveform vok and iok in unbalanced load

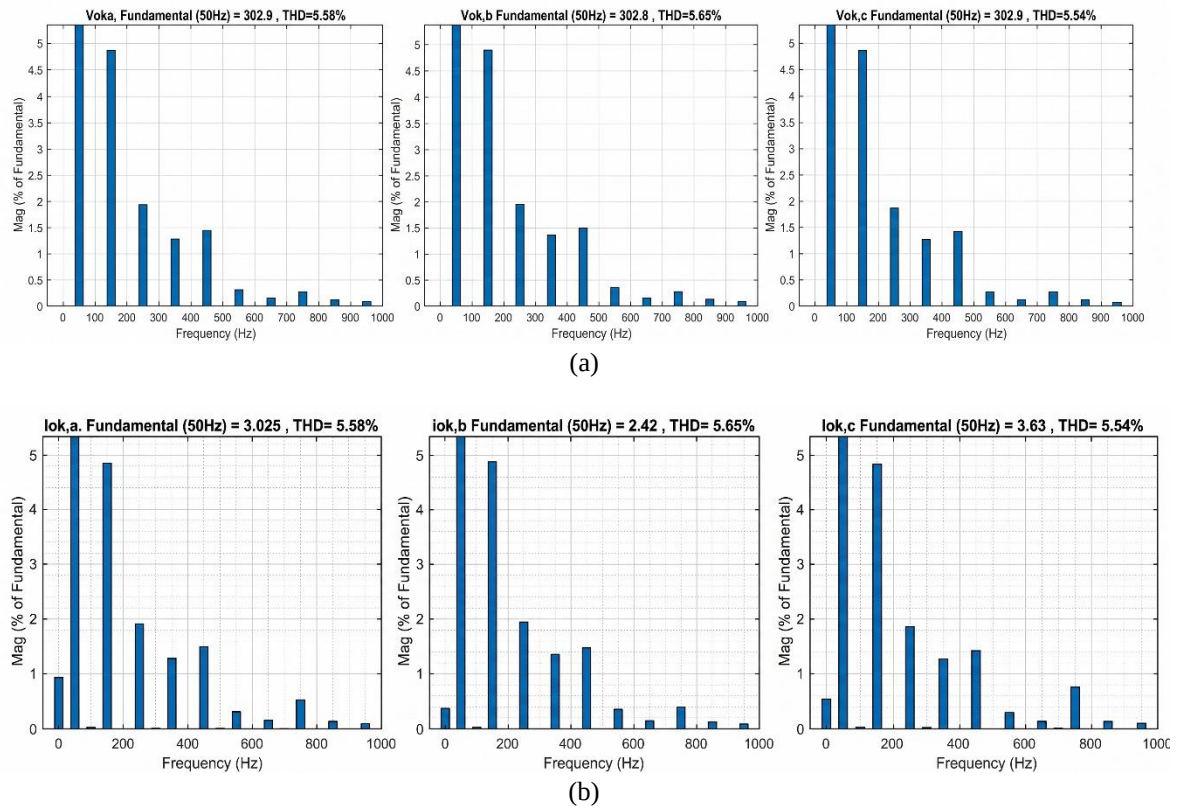


Figure 9. Harmonic spectrum and THD; (a) voltage and (b) current

3.5. Comparative analysis with previous studies

To better position the obtained results within the existing literature, the performance of the proposed method is compared with several representative studies on predictive control of multilevel inverters. Table 4 summarizes the main characteristics and harmonic performance reported in related works.

The results indicate that the proposed approach achieves very low harmonic distortion under ideal operating conditions while maintaining stable operation under realistic disturbances. The extremely low THD observed in the baseline scenario can be attributed to the seven-level CHB inverter's multi-level voltage synthesis capability, combined with predictive switching-state selection.

From a technical perspective, several factors influence the observed performance. First, the use of a voltage-centric cost function enables accurate tracking of the capacitor-voltage reference, directly improving voltage-waveform quality. Second, the seven-level voltage synthesis reduces harmonic distortion compared to lower-level inverter configurations. Third, the second-order reference extrapolation effectively compensates for the one-sample delay introduced by digital control implementation.

Under disturbed conditions, such as dc-link voltage sag and load imbalance, THD increases to approximately 5%. This increase is mainly due to switching vector quantization and to the interaction between the LCL filter dynamics and the predictive control decision process. Nevertheless, the controller maintains stable operation and preserves a PF close to unity, demonstrating the robustness of the proposed control strategy.

Although the proposed control strategy demonstrates excellent performance under the tested scenarios, several limitations should be acknowledged. First, the voltage-centric cost function may lead to clustering of switching states near the zero-crossing region, which may increase switching activity. Second, the use of a reduced switching set introduces quantization effects that may contribute to harmonic distortion under severe disturbances. Finally, the current implementation does not include active damping for the LCL filter, which could further improve stability under grid-connected conditions.

Table 4. Comparison with the other research

Author	Control method	Inverter type	Reported THD (%)
Ramirez <i>et al.</i> [13]	FCS-MPC	CHB inverter	1–2
Easley <i>et al.</i> [15]	Hierarchical MPC	Cascaded multilevel inverter	<1
Harbi <i>et al.</i> [17]	Reduced-complexity MPC	Multilevel inverter	0.8–1.5
This work	FCS-MPC+reference extrapolation	7-level CHB inverter	0.01 (ideal case)

4. CONCLUSION

This study investigated the performance of FCS-MPC applied to a three-phase seven-level CHB inverter with an LCL filter. The simulation results demonstrate that the proposed controller achieves excellent power quality under ideal operating conditions, with voltage THD below 0.1% and a PF close to unity. The controller is able to track the voltage reference accurately while maintaining stable switching behavior.

From a practical perspective, the results indicate that predictive control combined with lightweight delay compensation can be effectively implemented for multilevel inverter applications. The use of second-order reference extrapolation enables the controller to mitigate the effect of a one-sample actuation delay typically encountered in digital control platforms, while maintaining stable operation under disturbances such as dc-link voltage sag and load imbalance.

However, this study has several limitations. The evaluation is currently limited to simulation-based analysis, and the effects of additional practical factors such as switching losses, thermal behavior, and real-time processor constraints have not yet been experimentally verified.

Future research will focus on experimental validation through PIL and HIL implementations, as well as extending the proposed control framework to grid-connected operation with synchronization and negative-sequence handling.

The main technical contributions of this study are summarized as follows; i) computationally efficient FCS-MPC formulation for three-phase 7-level CHB inverter using full candidate evaluation framework, ii) integration of second-order reference extrapolation to compensate for one-sample actuation delay without increasing the algorithmic complexity, iii) a hardware-aware evaluation framework incorporating nonidealities, such as dead time, sensor noise, and dc-link disturbances, and iv) a comprehensive robustness analysis under dc-link voltage sag and load imbalance demonstrated stable operation and acceptable harmonic performance. These contributions provide a practical pathway toward the real-time implementation of predictive control in multilevel inverter systems.

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AUTHOR CONTRIBUTIONS STATEMENT

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Risnandar														
Imam Taufiqurrahman	✓		✓		✓				✓		✓		✓	✓
Rizal Ansor			✓	✓	✓			✓	✓		✓			
Miftahul Huda Pratama		✓				✓	✓			✓	✓	✓	✓	✓
Muhammad Lutfi		✓	✓			✓	✓	✓		✓				
Azhari														

C : Conceptualization	I : Investigation	Vi : Visualization
M : Methodology	R : Resources	Su : Supervision
So : Software	D : Data Curation	P : Project administration
Va : Validation	O : Writing - Original Draft	Fu : Funding acquisition
Fo : Formal analysis	E : Writing - Review & Editing	

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest. The funding agencies had no role in the study design, data collection and analysis, decision to publish, or preparation of the manuscript.

DATA AVAILABILITY

The data that support the findings of this study are available upon request from the corresponding author, [initials: AA]. The data, which contain information that could compromise the privacy of the research participants, are not publicly available due to certain restrictions.

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