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A novel 19-level inverter topology based on a single direct current source and reduced component count

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ABSTRACT

Conventional multilevel inverters (MLI) provide low harmonic distortion but often require many switches, passive components, and voltage sensors, increasing cost, size, and control complexity. This paper proposes a compact 19-level modified split-packed U-cell (MSPUC) inverter powered through one independent direct current (DC) supply source. The proposed configuration employs a reduced number of switches and only three capacitors. Its key contribution is the natural self-balancing of capacitor voltages under sensorless open-loop pulse width modulation (PWM) operation, eliminating the need for additional voltage sensors or auxiliary balancing circuits. In addition, the topology achieves a total standing voltage per unit (TSV_{pu}) of 4.22 and a cost function (CF) of 1.70, indicating reduced voltage stress and improved structural efficiency. MATLAB/Simulink simulations are performed under steady-state conditions, load variations, nonlinear loading, switching-frequency variation, and sudden DC-source disturbances. The obtained results confirm stable capacitor voltage regulation, fast dynamic response, and high-quality output waveforms. Under the nominal condition of R=20 Ω and L=20 mH, the load current total harmonic distortion (THD) is limited to 0.96% without using any external filter. Therefore, the proposed MSPUC inverter provides a compact, cost-effective, and low-complexity solution for efficient power electronic conversion systems.

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1. INTRODUCTION

The evolution of power electronics has shown that traditional two-level inverters are characterized by several weak points [1]. Modern applications require very high output power, characterized by a high-quality form of alternative energy [2]. This requirement applies to renewable energy systems and electric vehicles [3]. The use of multilevel inverters (MLI) in high-voltage industrial applications makes it possible to obtain a very low total harmonic distortion (THD); consequently, the inverter produces a high-quality waveform [4].

In recent years, several works have focused particularly on developing classic MLI configurations, such as the fixed neutral point clamped (NPC) inverter, the flying capacitor (FC) inverter, and the cascaded H-bridge (CHB) inverter [5]. However, these conventional approaches present a major challenge, which is manifested by the use of a large components in order to produce a high-quality voltage, characterized by a higher number of levels [6]. This major challenge has prompted researchers to develop new MLI configurations based on existing structures in the literature [7]. While using fewer switches helps reduce cost

and control complexity, it can create higher voltage stress (TSV) on individual switches [8]. This increases the maximum voltage stress and leads to greater switching losses, ultimately hurting the inverter's performance. These challenges have pushed researchers to explore innovative MLI designs, often called next-generation topologies [9]. Several important studies from the literature are worth examining for their key contributions.

To produce a high-quality output voltage, it is generally necessary to use several electronic components and several direct current (DC) power supplies [10]. This remains one of the major challenges of MLI. The use of several DC sources influences the complexity and cost. To address this challenge, researchers have proposed structures based on switched capacitors and several DC sources [11]. However, in many industrial applications, it is recommended to use only a single DC source, such as in electric vehicles. Indeed, the challenge of using a single source has led to the development of new MLIs with switched capacitors based on a single source [12]. These inverters use capacitors controlled either in open loop or closed loop to create several voltage levels.

In this context, the packed U-cell (PUC) topology [13] presents a competitive topology for MLI; it is characterized by the use of a single DC source and a few switched capacitors to generate a multilevel voltage. This new approach allows for the production of a voltage characterized by a very low THD through a reduced number of electronic components. On the other hand, this topology allows for managing the TSV applied to switches. It features a hybrid architecture that merges the advantages of both the CHB and the FC topologies. Overall, this architecture presents several practical advantages, especially a reduction in inverter costs and system reliability [14]. However, a significant challenge remains: regulating the auxiliary capacitor voltages, which requires a dedicated controller to maintain voltage balance. Certain PUC topology variants enable self-balancing through redundant switching states [15], [16]. This approach simplifies the overall system architecture by removing the need for extra control circuitry. On the other hand, many PUC inverter configurations require closed-loop control using voltage and current sensors; in fact, using external circuits for control leads to a higher inverter cost, and therefore, the system becomes complex [17].

To address the limitations that exist in current MLI topologies, a new 19-level topology referred to as modified split-packed U-cell (MSPUC) has been designed through the application of the PUC theory. The greatest contribution that characterizes the topology is the low-cost function (CF), which constitutes the primary contribution of this research paper. Due to its low CF, small size, and use of one DC power source, it makes the topology ideal for numerous energy conversions, such as photovoltaic cells, electric vehicles, and smart grids. The contributions of this paper are as follows:

- The development of a compact 19-level inverter topology, characterized by a reduced number of electronic components and a minimal normalized total standing voltage per unit (TSV_{pu}).
- The application of simple sensorless pulse width modulation (PWM) control ensures natural capacitor self-balancing.
- The generation of a high-quality output voltage with low THD, without using output filters.

2. METHOD

2.1. Circuit configuration and operating modes

Figure 1 summarizes the transition from the basic SPUC inverter to the proposed extended topology. The proposed inverter is derived from the SPUC inverter topology [18] shown in Figure 1(a). This configuration enables a nine-level output voltage using seven switches, including a unique DC input source associated with two capacitors. The proposed topology, illustrated in Figure 1(b), comprises a single DC source, eleven switches including one bidirectional switch, and three capacitors. Adding a capacitor and four additional switches to the basic SPUC topology enabled a 19-level output voltage to be delivered.

The innovative MSPUC design uses a well-adopted combination of three capacitors with the DC input source to create 19 different voltage levels with automatic balancing of the three capacitor voltages. The system connects the DC source with the three capacitors using commutation switches, allowing for precise control over the output levels. The capacitor voltage balancing mechanism results from the sequence of switching states imposed by the PWM strategy, which naturally alternates the charging and discharging phases of each capacitor, as shown in Table 1. Thus, over one operating cycle, the average energy exchange remains globally balanced, which keeps the capacitor voltages close to their desired values. When tested with V_{dc}=8E, the circuit shows impressive self-regulating behavior in open-loop operation, where the voltages naturally settle at $V_{C1}=V_{C2}=V_{dc}/4=2E$ and $V_{C3}=V_{dc}/8=E$, proving that the circuit can maintain proper voltage distribution while producing all 19 voltage levels as detailed in Table 1.

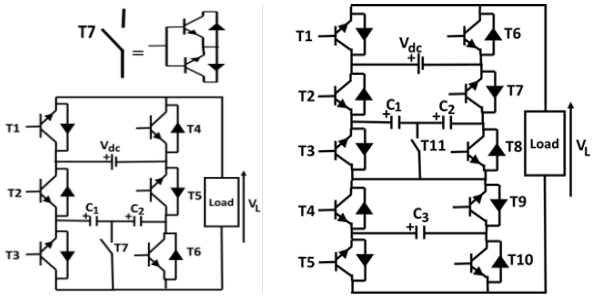


Figure 1. Circuit configurations of the proposed inverter topology: (a) SPUC inverter and (b) proposed MSPUC inverter

Table 1. Operating and switching states for the MSPUC inverter

State	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	C_1	C_2	C_3	V_L
1	1	0	0	1	0	0	1	1	0	1	0	Noef	Noef	DIS	9E
2	1	0	0	0	0	0	1	1	1	1	0	Noef	Noef	Noef	8E
3	1	0	0	0	1	0	1	1	1	0	0	Noef	Noef	CH	7E
4	1	0	0	0	0	0	1	0	1	1	1	Noef	CH	Noef	6E
5	1	0	0	0	1	0	1	0	1	0	1	Noef	CH	CH	5E
6	1	1	0	0	0	0	0	1	1	1	0	DIS	DIS	Noef	4E
6'	1	0	1	1	1	0	1	0	0	0	0	CH	CH	Noef	4E
7	1	1	0	1	0	0	0	0	0	1	1	DIS	Noef	DIS	3E
8	1	1	0	0	0	0	0	0	1	1	1	DIS	Noef	Noef	2E
9	1	1	1	1	0	0	0	0	0	1	0	Noef	Noef	DIS	E
10	1	1	1	1	1	0	0	0	0	0	0	Noef	Noef	Noef	0
10'	0	0	0	0	0	1	1	1	1	1	0	Noef	Noef	Noef	0
11	0	0	0	0	1	1	1	1	1	0	0	Noef	Noef	DIS	-E
12	0	0	0	0	0	1	1	0	1	1	1	Noef	DIS	Noef	-2E
13	0	0	0	0	1	1	1	0	1	0	1	Noef	DIS	DIS	-3E
14	0	0	1	1	1	1	1	0	0	0	0	DIS	DIS	Noef	-4E
14'	0	1	0	0	0	1	0	1	1	1	0	CH	CH	Noef	-4E
15	0	1	0	1	0	1	0	0	0	1	1	CH	Noef	CH	-5E
16	0	1	0	0	0	1	0	0	1	1	1	CH	Noef	Noef	-6E
17	0	1	1	1	0	1	0	0	0	1	0	Noef	Noef	CH	-7E
18	0	1	1	1	1	1	0	0	0	0	0	Noef	Noef	Noef	-8E
19	0	1	1	0	1	1	0	0	1	0	0	Noef	Noef	DIS	-9E

Noef: no effect, CH: charging, and DIS: discharging.

In the suggested 19-level inverter, the output voltage levels are obtained through a coordinated sequence of switching states, as illustrated in Figure 2 (in Appendix). In state 10, the circuit generates a zero output voltage by activating switches T_1, T_2, T_3, T_4, and T_5 as shown in Figure 2(a). In state 9, the output is equal to E by the activation of switches T_1, T_2, T_3, T_4, and T_{10} as illustrated in Figure 2(b); in this state, the capacitor C_3 is discharging. In state 8, the level 2E is obtained by the conduction of T_1, T_2, T_9, T_{10}, and T_{11} as shown in Figure 2(c); it is worth noting that in this state, the capacitor C_1 is in a discharge cycle. In state 7, the output voltage obtained is 3E by activating the switches T_1, T_2, T_4, T_{10}, and T_{11} as depicted in Figure 2(d); in this state, the capacitors C_1 and C_3 are in a discharge cycle. In state 6, the switches T_1, T_2, T_8, T_9, and T_{10} are activated to generate the level 4E as presented in Figure 2(e), resulting in the discharge of both C_1 and C_2. In state 5, the level 5E is reached by activating the switches T_1, T_5, T_7, T_9, and T_{11} as shown in Figure 2(f); in this state, the capacitors C_2 and C_3 are in the charging mode. In state 4, the inverter produces a voltage equal to 6E by activating T_1, T_7, T_9, T_{10}, and T_{11} as presented in Figure 2(g); in this state, the capacitor C_2 is in the charging cycle. State 3 yields 7E by activating T_1, T_5, T_7, T_8, and T_9 as shown in Figure 2(h); in this state, the capacitor C_3 is in a charging cycle. In state 2, an 8E output is generated through the operation of T_1, T_7, T_8, T_9, and T_{10} as demonstrated in Figure 2(i). In state 1, the inverter reaches its maximum output of 9E with the activation of T_1, T_4, T_7, T_8, and T_{10} as shown in Figure 2(j); in this state, the capacitor C_3 is in the discharging mode. The negative half-wave switch states are symmetrically listed in Table 1, including redundant states that enable sensorless automatic capacitor voltage balancing.

2.2. Capacitor design

One of the main challenges of MLI is the voltage drift of floating capacitors. This effect calls for a special approach to control the system to maintain balance in most cases. In order to address this issue in the suggested 19-level MLI configuration, the balancing is achieved automatically without requiring any

additional components. Nevertheless, the efficiency of the circuit under consideration is still influenced by the voltage ripples caused by the charging and discharging cycles of the capacitors. To ensure a satisfactory output voltage, this ripple must generally be kept between 5% and 10%. As shown in Figure 3, the amplitude of this variation depends primarily on the capacitance, the discharge current, and the maximum discharge duration (MDP). The sizing of the capacitors must therefore be based on a precise analysis of the operating sequences and current constraints. The peak-to-peak ripple of the voltage of capacitor C_i based on the load current is expressed by (1):

$$\Delta vc_i = \frac{\Delta Qc_i}{c_i} = \frac{1}{c_i}\int_{ta}^{tb} i_L(t)dt \quad (1)$$

The capacitance C_i is designed to maintain the voltage ripple within the prescribed limits, according to (2):

$$C_i = \frac{1}{\Delta vc_i}\int_{ta}^{tb} i_L(t)dt \quad (2)$$

The capacitor values of C_1, C_2, and C_3 required to satisfy the prescribed voltage ripple limits are determined as (3) to (5):

$$C_1 = \frac{1}{\Delta vc_1}\int_{t2}^{t4} i_L(t)dt \quad (3)$$

$$C_2 = \frac{1}{\Delta vc_2}\int_{t20}^{t22} i_L\,(t)\,dt \quad (4)$$

$$C_3 = \frac{1}{\Delta vc_3}\int_{t9}^{t10} i_L\,(t)\,dt \quad (5)$$

The capacitance values were derived from (3)–(5) by imposing a voltage ripple limit below 10% for an R–L load (20 Ω, 20 mH). The selected values, C_1=C_2=3000 µF and C_3=4000 µF, ensure stable capacitor voltages with limited ripple under all operating conditions.

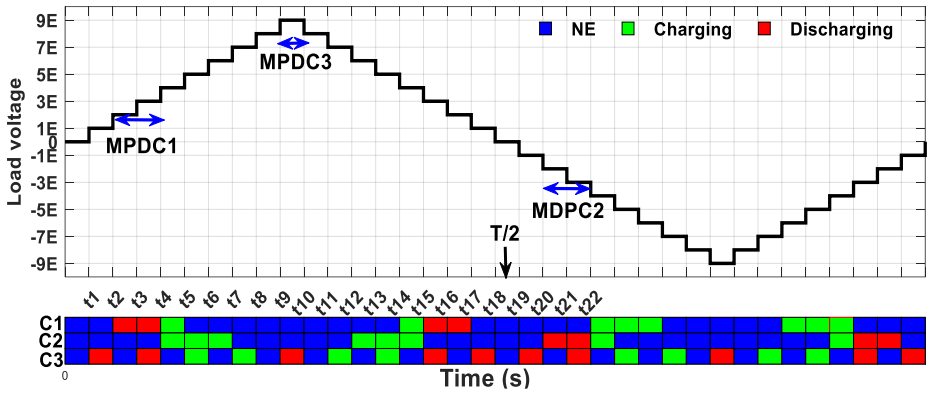


Figure 3. Load voltage waveform during capacitor charging and discharging

2.3. Voltage stress

The proposed MSPUC inverter uses eleven switches, one of which is bidirectional. The off-state voltage of each switch depends on the operating state. The voltage stress for each switch is as (6)-(9):

$$V_{T1} = V_{T6} = V_{dc} \quad (6)$$

$$V_{T2} = V_{T3} = V_{T7} = V_{T8} = V_{C1} + V_{C2} \quad (7)$$

$$V_{T11} = V_{C1} = V_{C2} \quad (8)$$

$$V_{T4} = V_{T5} = V_{T9} = V_{T10} = V_{C3} \quad (9)$$

The total blocking voltage (TBV) [19] experienced by the switches is defined as (10):

$$TBV = 2V_{dc} + 4(V_{C1} + V_{C2}) + V_{C1} + 4V_{c3} \quad (10)$$

Based on the selected voltage proportion values, V_{dc}=8E, V_{C1}=V_{C2}=2E, and V_{c3}=E, the TBV is calculated as (11):

$$TBV = 38E \quad (11)$$

2.4. Voltage gains of the modified split-packed U-cell inverter

The voltage gain of the MSPUC configuration is expressed as (12):

$$G = \frac{V_{max}}{V_{dc}} = 1.13 \quad (12)$$

2.5. Control approach for the modified split-packed U-cell inverter

The proposed MSPUC inverter employs a PWM control technique designed to maintain automatic voltage balance across the capacitors without employing current or voltage sensors. The working principle consists of comparing multiple triangular carrier signals with a sinusoidal reference waveform to generate the switching signal R(t) that governs the inverter's switches. Through this modulation process, the capacitors undergo periodic charging and discharging cycles. Additionally, the use of redundant switching states allows the inverter to self-balance the capacitor voltages around their reference levels. Figure 4 presents the proposed PWM technique and the corresponding control signal generation. Specifically, Figure 4(a) illustrates the PWM technique employed, while the control signal R(t) generated through this technique is illustrated in Figure 4(b). The electrical schematic illustrating the proposed modulation technique is shown in Figure 5.

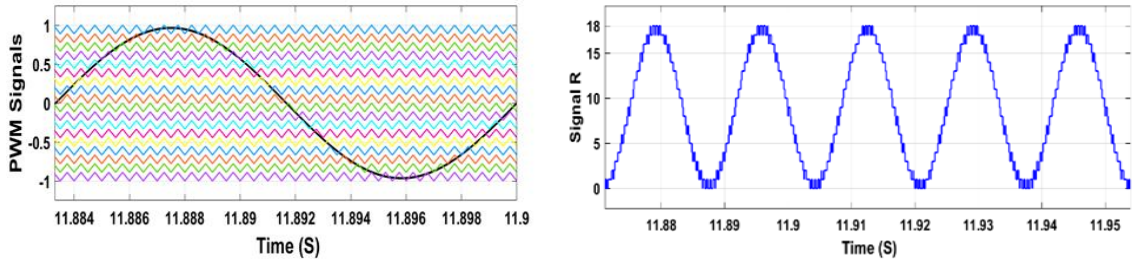


Figure 4. PWM control of the proposed inverter: (a) carrier-based sinusoidal modulation and (b) control signal (R(t))

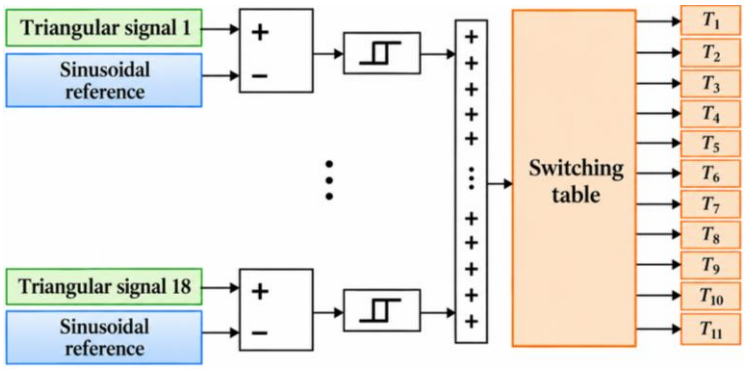


Figure 5. Electrical schematic of the proposed modulation technique

2.6. Comparative study

An in-depth comparative evaluation is performed based on the indicators that reflect the performance and cost of MLI. The evaluation metrics include the number of DC sources (N_{dc}), N_{SW}, the number of diodes (N_d), the number of output voltage levels (N_L), the number of gate drivers (N_{Gd}), and the

number of capacitors (N_C), as well as TSV_{pu} [20]. These parameters are used in a CF that allows comparing the topologies proposed in the literature. The CF used in the evaluation is defined by (13) [20]:

$$F_c = \frac{(N_{sw}+N_d+N_{Gd}+N_c+\alpha TSVpu\ ).N_{dc}}{N_L} \quad (13)$$

The TSV_{pu} of the MSPUC inverter is presented by (14):

$$TSVpu = \frac{TBV}{V_{max}} = \frac{38E}{9E} = 4.22 \quad (14)$$

Reducing the number of components improves the compactness of the topology and lowers the implementation cost, but it may also increase the voltage stress on some semiconductor devices. However, under the proposed design architecture, the aforementioned tradeoff still works out well, as seen from the small value of TSV_{pu} at 4.22, which means that the decrease in components is not done in exchange for increased stress on the voltage. Thus, the proposed MSPUC inverter proves to be a good combination of reduced component count and electrical performance.

The second characteristic that can be taken into consideration when evaluating inverter characteristics is the number of devices per voltage level (F_L), which can be determined as (15):

$$F_L = \frac{N_{sw}+N_d+N_c+N_{dc}}{N_L} \quad (15)$$

The component count for each voltage level (F_L) represents the number of active electronic components used per voltage level. This parameter should be used in the comparison because it presents a key factor in evaluating the cost and complexity of MLI.

Table 2 presents a detailed comparison between the MSPUC inverter and several MLI topologies recently proposed in the literature (2021–2025), including 7-level, 13-level, and 19-level configurations. The comparative analysis is based on the previously described parameters to examine the CF of each proposed configuration and the number of electronic components per level (F_L). It is worth noting that the CF is evaluated for two weighting factors, α=0.5 and α=1.5, as shown in Table 2. Based on CF, TSV_{pu}, and F_L indicators, the proposed inverter is characterized by a compact design; the MSPUC inverter configuration decreases the cost metric and the voltage constraint.

Table 2. Comparative study with existing configurations

Topology	Year	N_L	N_{dc}	N_c	N_{sw}	N_{Gd}	N_d	TSV_{pu}	F_L	CF(α=0.5)	CF(α=1.5)
[21]	2022	7	1	1	8	8	0	8	1.43	3	4.14
[22]	2021	7	1	3	9	9	2	4.30	2.14	3.59	4.21
[20]	2025	7	1	2	8	8	2	5.67	1.86	3.26	4.07
[23]	2021	13	2	4	14	14	2	5.67	1.69	5.67	6.54
[24]	2021	13	1	3	13	13	2	5.33	1.46	2.59	3.08
[25]	2021	13	1	3	13	13	2	5.16	1.46	2.58	2.98
[26]	2024	17	1	3	11	11	1	7	0.94	1.74	2.15
[27]	2022	17	2	1	11	11	2	6.75	0.94	3.28	4.07
[28]	2022	19	2	2	12	10	1	6.66	0.89	2.98	3.68
[29]	2025	19	2	3	14	12	3	4.67	1.16	3.61	4.11
Proposed	**2026**	**19**	**1**	**3**	**12**	**11**	**0**	**4.22**	**0.84**	**1.48**	**1.70**

3. RESULTS AND DISCUSSION

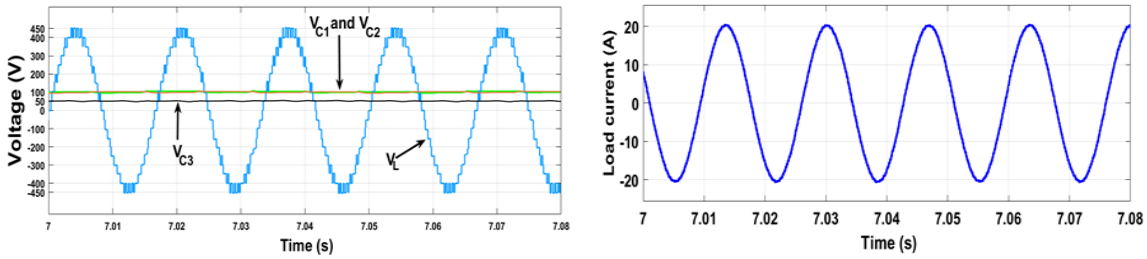
To validate the effectiveness of the MSPUC inverter under PWM operation, a set of simulations was conducted in MATLAB/Simulink. Initially, tests were conducted under fixed operating parameters to establish the nominal performance. The operating conditions were then modified in order to assess the performance of the control method in different scenarios.

3.1. Simulation under fixed parameters

Table 3 provides a summary of the parameters used in the simulation. The waveforms generated by the suggested inverter are shown in Figure 6, and include the load voltage, capacitor voltages, and load current waveforms. Figure 6(a) depicts the behavior of the capacitor voltages to converge to their respective references. V_{C1} and V_{C2} settle to a value close to one-quarter of the DC-link voltage V_{dc}, whereas V_{C3} converges to a value close to one-eighth. The same figure represents the output voltage V_L generated by the MSPUC inverter that consists of eighteen levels. Figure 6(b) illustrates the corresponding load current, which exhibits excellent sinusoidal quality.

Table 3. Simulation sittings

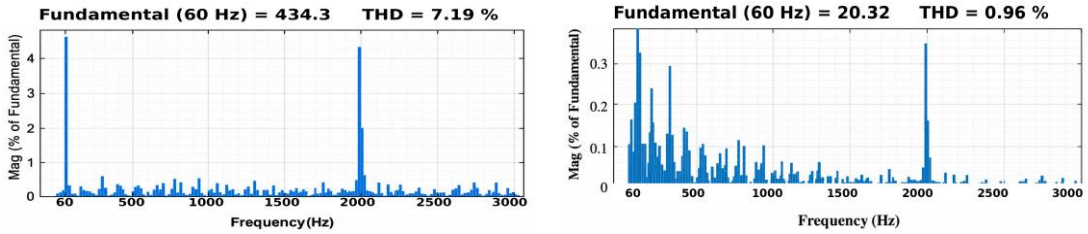
Parameters	V_{dc} (V)	R (Ω)	L (mH)	C_1 (uF)	C_2 (uF)	C_3 (uF)	Switching frequency f (Hz)	Modulation index
Values	400	20	20	3000	3000	4000	2000	1



(a) (b)

Figure 6. Dynamic response of the proposed inverter under load variation: (a) load voltage V_L and capacitor voltages V_{C1}, V_{C2}, and V_{C3} and (b) load current

The excellent quality of the load voltage and load current waveforms is confirmed by the THD values shown in Figure 7. Indeed, the voltage THD reaches 7.19% (Figure 7(a)), while the current THD is limited to 0.96% (Figure 7(b)). The observed THD is very low for both voltage and current. The low THD achieved in open-loop operation is primarily attributed to the 19-level output voltage waveform, which closely approximates a sinusoidal shape and inherently limits low-order harmonics. Furthermore, the self-balancing behavior of capacitor voltages ensures the accuracy of the generated voltage levels.



(a) (b)

Figure 7. FFT analysis of the inverter: (a) load voltage spectrum and (b) load current spectrum

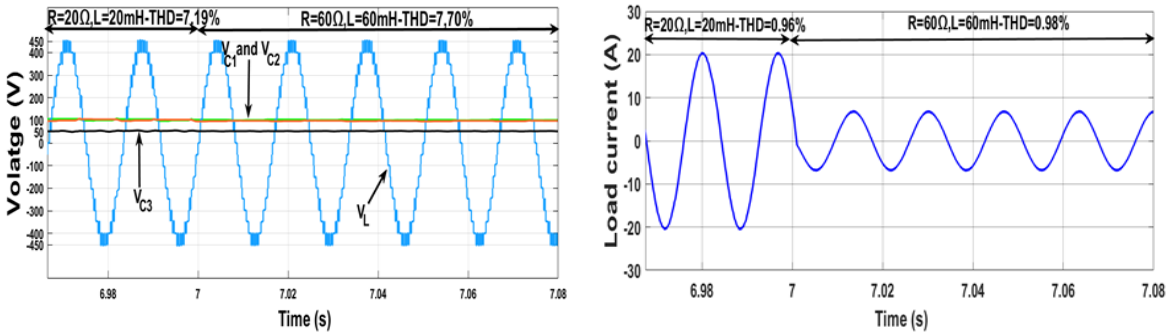
3.2. Operation under varying load conditions

Another simulation was carried out to study the transient response of the 19-level MSPUC inverter when the load conditions were altered. This alteration occurred at t=7 seconds, where the load resistance was increased from 20 Ω to 60 Ω, and the inductance was increased from 20 mH to 60 mH, while all other parameters remained unchanged. Figure 8 shows the waveforms of the load voltage, capacitor voltages, and load current. As shown in Figure 8(a), the capacitor voltages quickly return to equilibrium after the disturbance. V_{C1} and V_{C2} settle at about one-quarter of V_{dc}, while V_{C3} stabilizes near one-eighth of V_{dc}. This voltage regulation maintains the 19-level output voltage before and after the load transition. Figure 8(b) shows that the load current preserves its quasi-sinusoidal waveform. The corresponding figures report the associated THD values; the THD analysis shows a slight increase, the voltage THD rises from 7.19% to 7.70%, while the current THD underwent only a slight variation. These limited variations demonstrate the robustness of the MSPUC inverter under different load conditions.

3.3. Performance under nonlinear load conditions

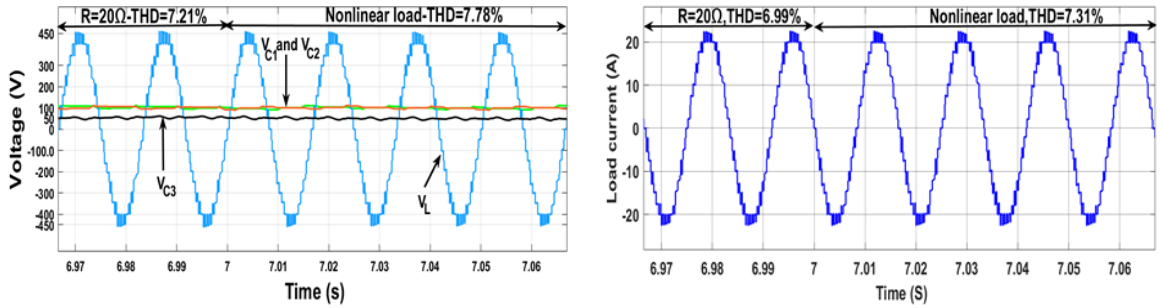
The stability analysis of the MSPUC inverter was performed in the case of a nonlinear load. Initially, the inverter supplies a resistive load; then, at t=7 s, the load is replaced by a nonlinear load through a diode rectifier. Figure 9 shows the load voltage, capacitor voltages, and load current waveforms. As observed in Figure 9(a), the three capacitor voltages remain close to their reference values after the sudden load change, indicating that the natural self-balancing mechanism is preserved. The output voltage also keeps its 19-level shape. Figure 9(b) shows that the load current remains nearly sinusoidal, although some distortion appears due to the nonlinear load. The THD results support this observation, since the voltage THD

increases only from 7.21% to 7.78%, while the current THD increases from 6.99% to 7.31%. These small variations show that the MSPUC inverter maintains robust performance under nonlinear load conditions.



(a) (b)

Figure 8. Waveforms during load change: (a) load voltage (V_L) and the capacitor voltages V_{C1}, V_{C2}, and V_{C3} and (b) load current



(a) (b)

Figure 9. Waveforms during nonlinear load operation: (a) load voltage (V_L) and the capacitor voltages V_{C1}, V_{C2}, and V_{C3} and (b) load current

3.4. Performance under direct current input fluctuation

The inverter was also evaluated under sudden DC source fluctuation. At t=7 s, the voltage V_{dc} was reduced from 400 V to 200 V. Figure 10 illustrates the load voltage response, the corresponding FFT analysis, and capacitor voltages during this transition. Before the change, the three capacitor voltages are stabilized around their predefined values, as shown in Figure 10(a). After a short transient interval, they converge to their new equilibrium points, as illustrated in Figure 10(b), allowing the inverter to maintain a high-quality 19-level output voltage with a voltage THD unchanged at 7.19%.

Figure 11 illustrates the load current waveform and corresponding FFT analysis under DC source variation. Figures 11(a) and (b) show the results before and after the variation, respectively. In both cases, the current remains sinusoidal, while the current THD remains constant at 0.96%, respectively, confirming preserved output power quality.

3.5. Performance under switching frequency variation

To evaluate the effect of switching frequency variation on the 19-level MSPUC inverter, a simulation was performed by increasing the switching frequency from 2000 Hz to 3000 Hz at t=7 s, while all other parameters remained unchanged. Figure 12 presents the load voltage, capacitor voltages, and load current waveforms. As shown in Figure 12(a), the capacitor voltages remain regulated around their reference values, and the load voltage preserves its 19-level waveform during this transition. Figure 12(b) shows that the load current remains nearly sinusoidal during this transition. The corresponding figures report the associated THD values, indicating improved harmonic performance as the voltage THD underwent a significant change, while the current THD underwent only a slight variation. These results confirm that increasing the switching frequency enhances the quality of the output waveforms.

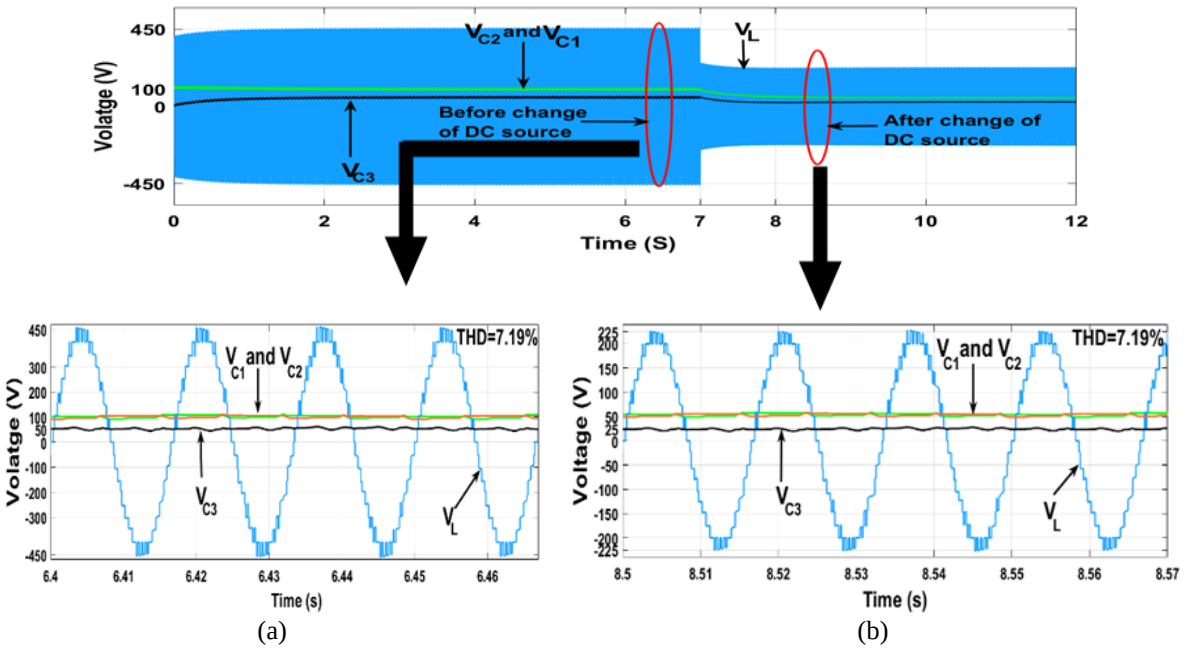


Figure 10. Waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{C2}, and V_{C3}): (a) before the change of the DC source and (b) after the change of the DC source

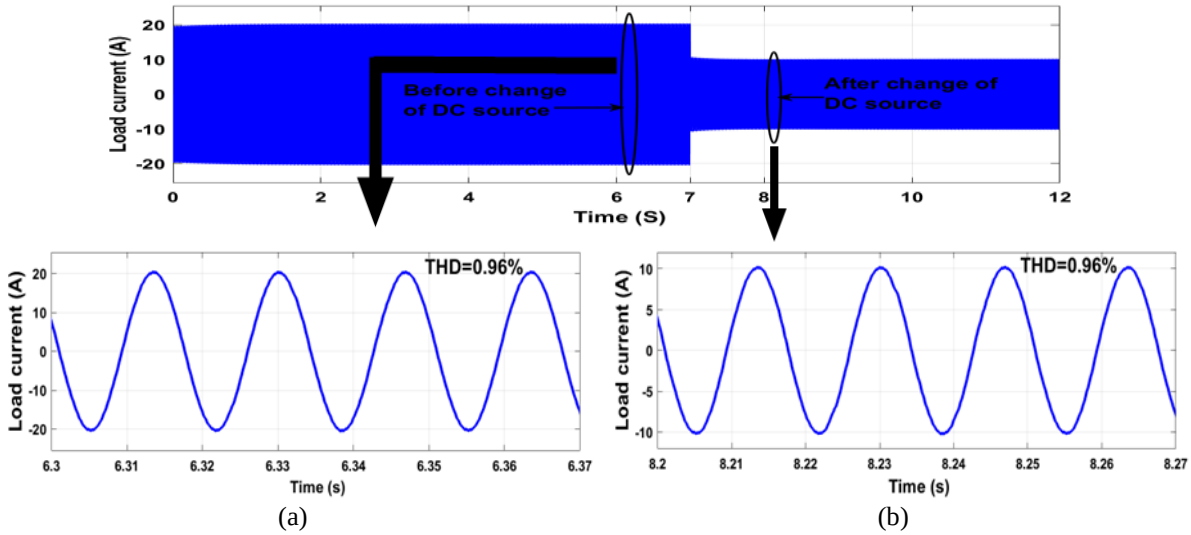


Figure 11. Load current waveform: (a) before and (b) after the DC source change

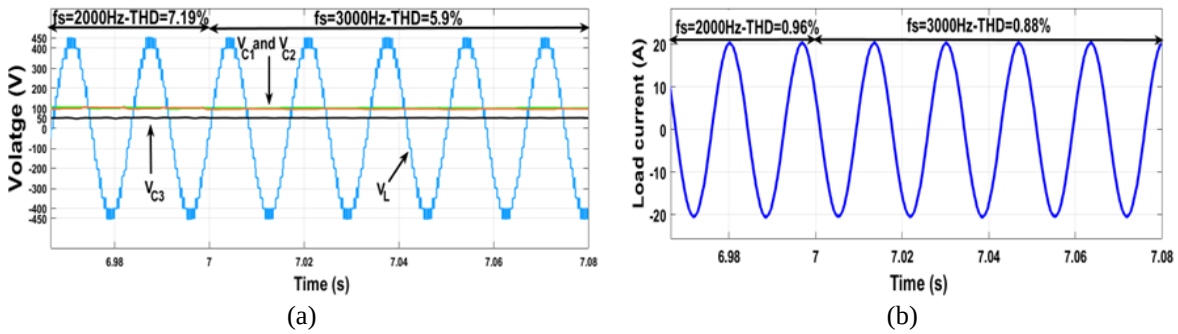


Figure 12. Waveforms under switching frequency variation: (a) load voltage V_L and capacitor voltages V_{C1}, V_{C2}, and V_{C3} and (b) load current

3.6. Statistical evaluation of total harmonic distortion

To evaluate the harmonic stability of the proposed inverter, a statistical analysis of the THD values obtained under various scenarios was performed. For n tests, the mean, variance, and standard deviation are given by (16) up to (18). These indicators allow us to quantify, respectively, the average THD level and its dispersion. Here, they are applied to the five THD values for voltage and current obtained.

$$Mean(THD) = \frac{1}{n}\sum_{i=1}^{n} THD_i \tag{16}$$

$$Var(THD) = \frac{1}{n}\sum_{i=1}^{n}(THD_i - Mean(THD))^2 \tag{17}$$

$$\sigma_{THD} = \sqrt{Var(THD)} \tag{18}$$

The corresponding statistical indicators are presented in Table 4. The results show that the proposed inverter maintains stable voltage harmonic performance under different operating conditions. The low variance (0.453) and standard deviation (0.673%) of the voltage THD confirm that the output voltage quality is only slightly affected by variations in the system parameters, demonstrating the robustness of the proposed topology. In contrast, although the current THD exhibits a lower average value (3.424%), its higher variance (9.267) and standard deviation (3.044%) indicate greater sensitivity to the load characteristics. This behavior is mainly attributed to the influence of resistive and nonlinear loads on the output current. Therefore, the statistical analysis confirms that the proposed inverter effectively preserves the output voltage quality while ensuring satisfactory current harmonic performance over a wide range of operating conditions.

Table 4. Statistical summary of THD results

THD parameters	Mean (%)	Variance	Standard deviation (%)
Load-voltage THD	7.156	0.453	0.673
Load-current THD	3.424	9.267	3.044

4. CONCLUSION

This work introduced an optimized 19-level inverter using a single DC source, with sensorless capacitor self-balancing, simple control, and high-quality output voltage. The suggested inverter has a compact and straightforward structure; thus, it can be applied to multiple applications, including photovoltaic systems, electric automobiles, and smart grids. In photovoltaic systems, it can help reduce the cost and simplify the converter structure. In electric vehicles, it can improve energy efficiency and lower switching losses. Therefore, this inverter offers a practical solution for modern energy conversion systems. Its ability to deliver high-quality power with a simple control scheme also makes it a promising candidate for modern intelligent grid infrastructures. From a hardware feasibility perspective, the use of a single DC source and a limited number of switches reduces the required sensing and control hardware. However, practical implementation requires selecting semiconductor switches with appropriate voltage and current ratings, using isolated gate driver circuits, and ensuring suitable dead-time control between complementary switches. Moreover, the reduced voltage stress indicated by the TSV_{pu} value facilitates the selection of commercially available power devices. However, despite these advantages, there are two weaknesses associated with this topology. The first is that the lack of common ground might make the implementation of this topology more difficult within the photovoltaic circuitry. Another weakness of the topology is that the voltage gain is quite low (G=1.17).

These limitations represent avenues for future research. In particular, a variant incorporating a common ground could be considered to facilitate the use of this topology in photovoltaic applications, while an improvement in voltage gain could be achieved by adding a step-up stage or by reconfiguring the structure. Furthermore, the use of a closed-loop model predictive control (MPC) is recommended to enhance the dynamic performance of the MSPUC inverter by reducing the settling time. It would also be relevant to conduct experimental validation under real operating conditions, as well as a thermal study based on the assessment of conduction and switching power losses.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Taoufiq El Ansari	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	
Ayoub El Gadari		✓		✓				✓	✓	✓		✓		
Youssef Ounejjar		✓		✓						✓		✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Simulation data can be provided by the corresponding author upon justified request.

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APPENDIX

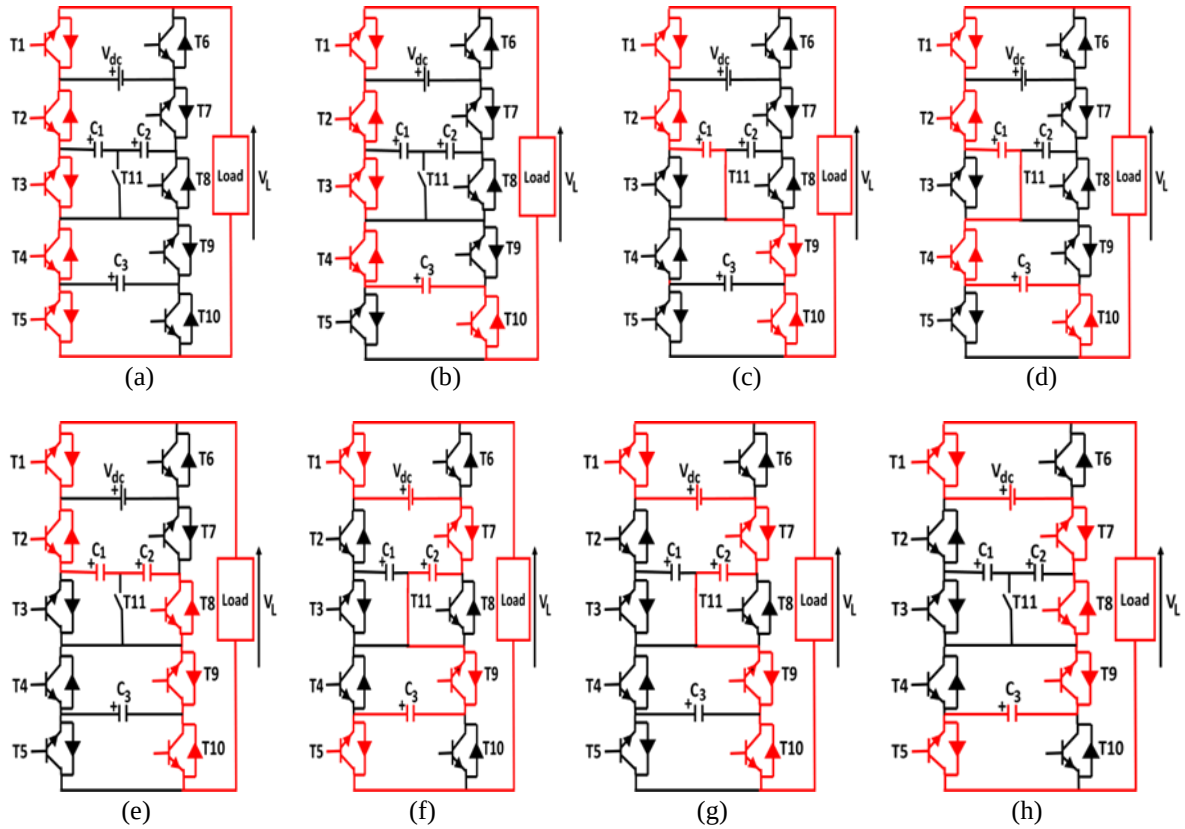


Figure 2. Different operating states for the MSPUC MLI topology: (a) V_L=0, (b) V_L=E, (c) V_L=2E, (d) V_L=3E, (e) V_L=4E, (f) V_L=5E, (g) V_L=6E, and (h) V_L=7E

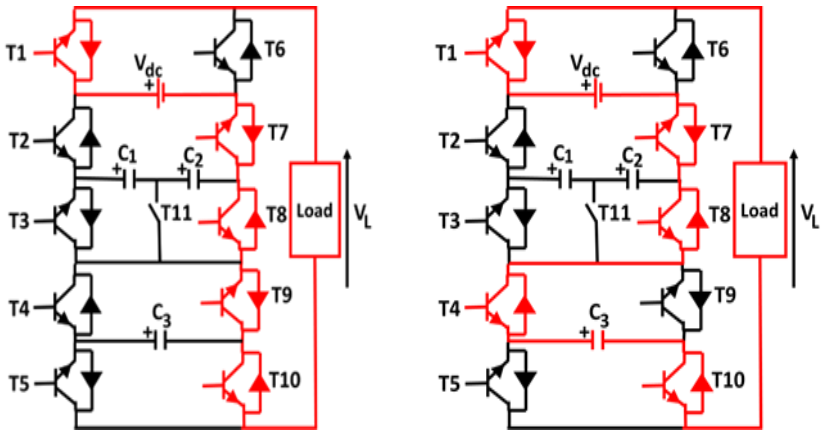


Figure 2. Different operating states for the MSPUC MLI topology: (i) V_L=8E and (j) V_L=9E *(continued)*

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