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Energy-efficient flip-flop design using sense amplifier and clock gating techniques for next-generation IoT nodes

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ABSTRACT

A clock-gated sense amplifier-based flip-flop (SAFF) that can operate dependably over a wide voltage and temperature range is suggested in the research paper. The proposed flip-flops (FF) drastically lowers the power and space requirements. Throughout all input data activity variations dependable and low-power operation is made possible by the single-ended latch design and the modified sense amplifier. The design utilization of the proposed SAFF which is made with 90 nm and 65 nm complementary metal-oxide-semiconductor (CMOS) technology is verified by a systematic and conclusive analysis using corner instance simulation for significant process, voltage, and temperature (PVT) variations. In addition, when the data is not changing a clock gating mechanism is employed to minimize the unwanted transition and lower power consumption. When SAFF and clock gated sense amplifier-based flip-flop (CGSAFF) are compared across various CMOS technologies the CGSAFF achieves a much lower delay than the traditional SAFF. The delay decreases from 47 to 6 ps in 90 nm technology and from 60 to 7 ps in 65 nm technology. This shows that CGSAFF outperforms SAFF in terms of speed performance and power efficiency making it more appropriate for portable internet of things (IoT) applications that require low power and high speed.

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1. INTRODUCTION

Smart applications in healthcare, wearable electronics, industrial automation, and wireless sensor networks have been made possible by the internet of things (IoT) explosive growth, enhancing operational effectiveness and quality of life [1]. However, in order to guarantee a long operational lifespan and sustainable resource utilization, battery-powered IoT devices need energy-efficient hardware. Furthermore, secure, dependable, and low-power circuit architectures are required by contemporary system-on-chip (SoC) platforms for wearable medical devices, biomedical implants, and portable edge systems [2].

In digital systems, flip-flops (FFs) are essential sequential components that offer temporary data synchronization and storage. These circuits greatly increase the overall chip area and dynamic power consumption of contemporary processors, which are made up of thousands of FFs [3]. Therefore, extending battery life and increasing energy efficiency in IoT applications requires lowering FF power consumption [4], [5]. Among different architectures, sense amplifier-based flip-flops (SAFFs) are appealing for low-power

complementary metal-oxide-semiconductor (CMOS) systems because they provide faster operation, quicker setup times, and less power than traditional master-slave FFs [6], [7].

Improved SAFF architectures [8] have been suggested by a number of researchers to improve delay performance and power efficiency. Multi-threshold complementary metal–oxide–semiconductor (MTCMOS)-based SAFFs maintained dependable operation below 0.4 V while reducing power consumption by 36.09% and clock-to-Q delay by 41.3% [9], [10]. Dual-edge triggered (DET-FFs) based on true single-phase clocking (TSPC) have been shown to operate reliably under wide process, voltage, and temperature (PVT) variations at supply voltages as low as 0.28 V [11], [12]. Similarly, optimized pulse-generation techniques allowed pulse-triggered FFs to significantly reduce power consumption and propagation delay [13]–[15]. While clock-based (CB-SAFF) architectures showed exceptional low-voltage performance for wireless sensor nodes and ultra-low-power IoT applications [16], [17], improved SAFF designs further improved the power-delay product (PDP) and switching efficiency under various data activities [18]–[20]. Despite these improvements, current clock-gating, and SAFF designs mainly maximize specific performance metrics like low-voltage operation, power, or delay. They are still less appropriate for energy-constrained IoT systems due to their needless internal switching activity, extra circuit overhead, or poor robustness under large PVT variations.

This work suggests a clock-gated sense amplifier flip-flop (CGSAFF) that combines an internal clock-gating mechanism with transistor-level optimization to overcome these drawbacks. Without requiring a large amount of hardware overhead, the suggested architecture reduces dynamic power consumption, propagation delay, and PDP by suppressing redundant switching activity. In order to show dependable operation, the design is also assessed under wide PVT variations across several complementary metal–oxide–semiconductor (CMOS) technology nodes. The suggested CGSAFF is especially well-suited for applications where ultra-low power consumption, fast operation, and reliable performance are crucial, such as wearable medical equipment, implanted biomedical sensors, wireless sensor nodes, smart meters, and portable edge computing platforms.

2. EXISTING METHOD

The sensing phase and the latching phase are the two main stages of operation for a basic SAFF. Architecture of CBSAFF system comprises a set–reset (SR) sensing stage and an SR latching stage, as illustrated in Figure 1. In order to create complementary signals set bar (SB) and reset bar (RB) that are applied to a slave latch for data storage, the sensing block uses a high-speed differential sense amplifier. The latch maintains its prior state during the pre-charge phase when the clock is low. The circuit evaluates the input during the high clock phase, pulling RB low for logic 0 and SB low for logic 1. When the clock edge rises, these signals dictate the final result. The CB-SAFF is regarded as an advanced SAFF architecture because of its high performance and reliable timing characteristics.

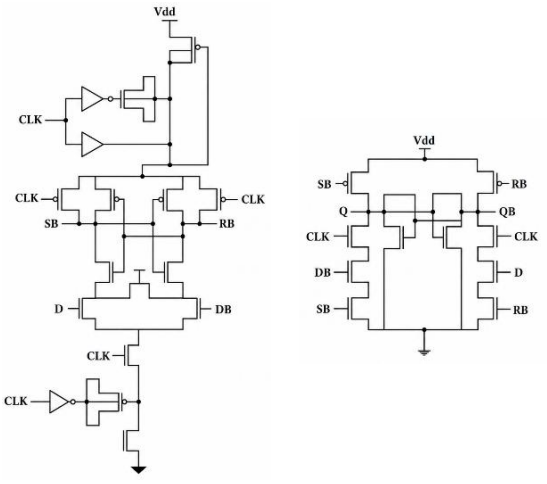

Figure 1. Architecture of CBSAFF using SR sensing and latch stage

The FF architecture presented in [21] employs a capacitive-boosted sensing stage using MOS devices as high-density capacitors. During the pre-charge phase (CLK=0), the boost capacitor stores charge, which is released during the evaluation phase (CLK=1) to increase the sensing node voltage. This charge boosting enhances the differential sensing margin, enabling reliable latch regeneration while minimizing clock loading. As a result, the design achieves robust operation, faster data amplification, and improved reliability under low-voltage conditions.

When the clock switches to logic 1 the barrier circuit described in [22] produces a controlled voltage-doubling effect to stop the clock network from driving a highly capacitive load. This method is shown in a schematic of the Strollo's SAFF (Figure 2). Its output stage allows the output to switch from high to low via an additional pull-down transistor network by combining the characteristics of an n-type (N-CMOS) sensing structure with a NAND-based SR latch. The design considerably lowers dynamic power dissipation by removing the speed-up circuitry and reducing the size of some transistors. Without sacrificing performance, the recognition (sensing) transistors can be further reduced thanks to the decrease in capacitive load. To reduce overall switching losses a PMOS device is integrated into the output stage to reduce crowbar current and enhance delay characteristics during the $1 \rightarrow 0$ transition. Jeong *et al*. [9] suggested a SAFF powered by a transition-completion (TC) signal in order to overcome the drawbacks of previous SAFF implementations under low-voltage operation. The complementary outputs of the sensing stage are the inputs of a NAND gate that generates the TC signal as illustrated in Figure 3. In order to ensure reliable data resolution even at lower supply voltages the TC node only discharges after the sensing stages SET output has completely transitioned.

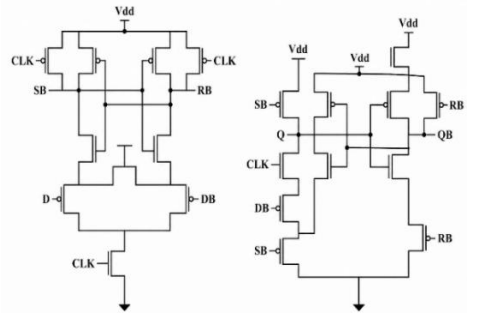

Figure 2. Architecture of Strollo's FF system using SR sensing and latch stages

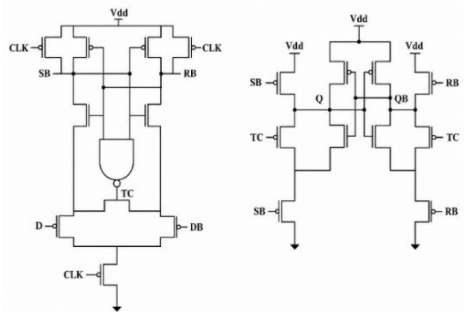

Figure 3. Architecture of Jeong's FF system using SR sensing and latch stages

As a result, the TC and SET nodes briefly rise when the clock changes from high to low creating a slight transient disturbance at the output. This glitch however is much less than what is seen in traditional SAFF implementations. Stable and dependable data regeneration is ensured by the architecture which successfully removes contention between the latching PMOS devices and the pull-down networks driving the output and its complement.

Nikolics SAFF which has a similar sense amplifier configuration and is shown in Figure 4 is an example of such a design. Small keeper transistors are used in these designs latching stage [23] where each output node has a single active transistor during state transitions. Both outputs have uniform propagation delays because the slave latchs true and complementary signal paths have a symmetric structure. External driver transistors can effectively update the latch state and drive the output load because the compact keeper transistors quickly shut off during transitions. This configuration keeps resistance to crosstalk during low clock pulses while streamlining the optimization of output transistor sizing. Additionally, it permits reduced clock swing operation and logic integration within the FF. Crowbar current is effectively eliminated by making sure that only one transistor conducts during switching increasing power efficiency and boosting the output stages drive capability. The updated N-C2MOS latches utilized in Kims suggested SAFF design are shown in Figure 5.

The sense amplifier in the conventional SAFF is the same [24], [25]. The additional capacitive loading that the cross-coupled inverters introduce at the output nodes is insignificant because they are implemented with minimum-sized transistors. Additionally, the differential nodes are completely decoupled which guarantees independent and quicker switching behavior because the load capacitance on one output node has no effect on the others transition speed. The CB-SAFF, one of the current SAFF architectures, offers robust operation and strong timing characteristics through distinct sensing and latching stages. Nevertheless, its differential sensing network still experiences significant switching activity, which raises dynamic power under frequent data transitions. By employing charge boosting, the capacitive-boosted SAFF in [21] increases sensing margin and permits dependable low-voltage operation; however, the additional boosting circuitry adds extra capacitive overhead and complicates the design. Although Strollo *et al*. [22] SAFF maintains high-speed operation while reducing dynamic power and crowbar current, the voltage-doubling barrier circuit complicates implementation and may make it more sensitive to process variations. Although Jeong *et al*. [9] TC SAFF successfully removes latch contention and enhances low-voltage reliability, the TC logic adds extra control circuitry and a temporary output glitch. Although Nikolic *et al*. [23] SAFF achieves symmetric propagation delay, lower crowbar current, and effective output driving, design optimization is more difficult because it depends on carefully sized keeper transistors. Although the cross-coupled latch structure increases the number

of transistors and area overhead, Kim *et al*. [24] SAFF, [25] provides decoupled differential nodes and faster switching with minimal loading. The proposed CGSAFF for energy-constrained IoT applications is motivated by the fact that previous SAFF designs, while improving speed, sensing reliability, or power efficiency, did not simultaneously minimize redundant switching activity, reduce power and delay, and maintain robust operation under wide PVT variations.

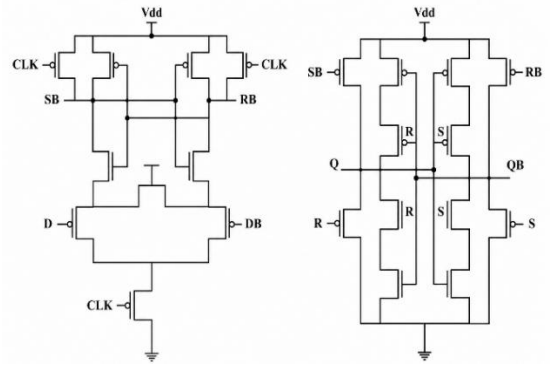

Figure 4. Architecture of Nikolic's FF system

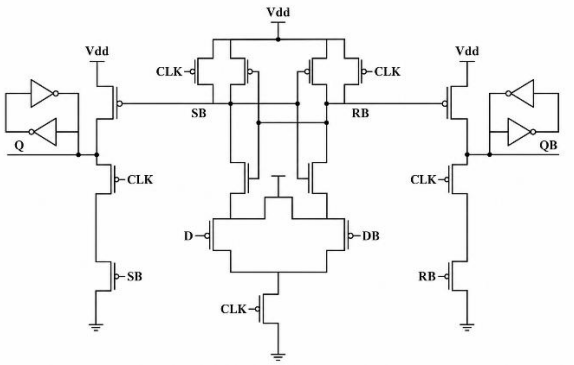

Figure 5. Architecture of Kim's FF system

3. PROPOSED METHOD

The proposed circuit was designed and verified using the Microwind 3.8 for transistor-level schematic design, layout generation, and post-layout simulation. DSCH 3.8 for logic verification and xilinx vivado design suite (version 2018.2) for field-programmable gate array (FPGA) synthesis and functional verification. The circuit was evaluated under the following operating conditions: supply voltages: 0.7 V, 0.8 V, 0.9 V, and 1.8 V, temperature: 27 °C (typical). Figure 6 (in Appendix) illustrates the overall implementation of the proposed CGSAFF, from transistor-level circuit design to register transfer level (RTL) realization for FPGA implementation. The proposed CGSAFF is shown in Figure 6(a). The proposed method introduces an energy-efficient SAFF with clock gating architecture for low-power IoT applications and extends its application to the design of an 8-bit counter. The architecture consists of three major components: an XOR-based activity detector (AD), a clock-gating unit, and a SAFF. The AD continuously compares the current input data with the previously stored value and generates an enable signal only when a change in the input data is detected. This enable signal controls the clock-gating circuitry, which allows clock pulses to reach the FF only during active data transitions, thereby suppressing unnecessary clock switching and reducing dynamic power consumption. The switching AD compares the present input data with the previously stored data using an exclusive OR (XOR) gate. The detector generates an activity signal only when a data transition occurs, thereby preventing unnecessary clock switching and reducing dynamic power consumption. The combinational logic depth is one XOR stage, resulting in a short critical path. The propagation delay of the detector consists of the register clock-to-Q delay and the XOR gate delay.

$$tPD = tCQ + tXOR$$

The sense amplifier array (SAA) acts as the storage element, offering high-speed operation with low power dissipation and minimal hardware overhead. To demonstrate the effectiveness of the proposed approach, an 8-bit counter was implemented using the clock-gated SAFF structure, where the counter state is updated only when the enable signal is asserted. The complete design was described using verilog hardware description language (HDL) and synthesized using Xilinx Vivado for FPGA implementation. Power and resource analyses were carried out to evaluate the efficiency of the architecture. The obtained results show that the proposed design achieves substantial reductions in dynamic power and junction temperature while requiring very few logic resources. Therefore, the integration of SAFF with clock-gating techniques provides an effective low-power solution for battery-operated IoT devices, wireless sensor networks, wearable electronics, smart sensors, and edge computing systems, making it highly suitable for next-generation energy-efficient digital platforms.

The suggested energy-efficient register file (RF) is implemented at the RTL as shown in the Figure 6(b). The three main components of the design are input/output interface buffers an XOR AD and a SAFF. Input buffers (IBUFs) allow the 8-bit input data bus d[7:0] clock signal (clk) and reset signal (rst) to enter the FPGA. To guarantee low-skew clock distribution throughout the design the clock signal is routed via a global clock buffer (BUFG). The xor_activity_detector block serves as a unit for detecting changes. It constantly contrasts the data that is being input with the data that has already been stored. The XOR logic

produces an activity detect (AD) signal whenever a bit transition is detected. This signal shows whether the incoming data is different from the data that already exists. The input data and the AD signal are sent to the SAFF block. The stored value is only updated by the SAFF when a data transition is identified. Dynamic power consumption is decreased by avoiding needless switching activity if the incoming data doesn't change. After passing through output buffers (OBUFs) the SAFFs output data is routed to the 8-bit output bus q[7:0]. These buffers give external connections the drive strength they require.

The RTL schematic of the proposed 8-bit CGSAFF Architecture and 8-bit CGSAFF based counter designs is displayed in Figure 6(c). The SAFF storage element is controlled by buffered clock and reset signals and the 8-bit output bus is driven by output buffers. For high-performance very large-scale integration (VLSI) and FPGA-based systems the straightforward architecture offers an effective low-power storage solution that requires few FPGA resources.

4. RESULTS AND DISCUSSION

Clock gating is a common power-saving technique used in VLSI circuits to reduce unnecessary switching activity in sequential elements. Clock gating reduces dynamic power consumption by allowing selective activation in response to control signals instead of FFs being toggled continuously with each clock pulse. Clock gating and SAFF are combined in the CGSAFF. Clock gating is integrated into the SAFF architecture of the CGSAFF to further improve power efficiency. Table 1 summarizes the performance analysis of the existing method.

Table 1. Performance analysis of existing method

Ref.	Layout area (μm^2)	No of transistors	PDP @ 0.7 V (µW)	PDP @ 0.8 V (µW)	PDP @ 0.9 V (µW)	C-Q delay @ 0.9 V (ps)
CBSAFF	0.316	38	159.698	70.594	127.457	56.22
Strollo *et al*. [22]	0.279	23	26.673	24.898	24.693	16.948
Jeong *et al*. [9]	0.247	26	33.916	27.874	17.84	13.424
Nikolic *et al*. [23]	0.262	28	34.061	26.155	31.431	26.408
Kim *et al*. [24]	0.352	26	62.971	66.685	72.239	30.065

The proposed CBSAFF was designed using 180 nm CMOS technology. The transistor dimensions were selected to provide a balance between propagation delay, power consumption, and layout area. Technology: 180 nm CMOS supply voltages: 0.7 V, 0.8 V, and 0.9 V threshold voltages (typical): NMOS: VTHN≈0.42 V and PMOS: VTHP≈−0.45 V transistor sizing:
NMOS: W/L=0.36 µm/0.18 µm.
PMOS: W/L=0.72 µm/0.18 µm.
Load capacitance: 10 fF at the output node.

A clock gating control circuit that selectively activates the sense amplifier stage only when necessary is used to achieve this. With the CGSAFF contemporary VLSI designs can benefit from a high-speed low-power solution. By integrating the advantages of sense amplifier-based latching and clock gating CGSAFF lowers power consumption without sacrificing functionality. Because of this it is the perfect option for energy-efficient computing systems memory circuits and microprocessors with power-sensitive applications. Clock gating is a major FF design advancement that SAFF incorporates guaranteeing that next-generation electronic systems achieve greater energy efficiency without compromising speed. Figures 7 and 8 displays the proposed SAFFs layout and simulation.

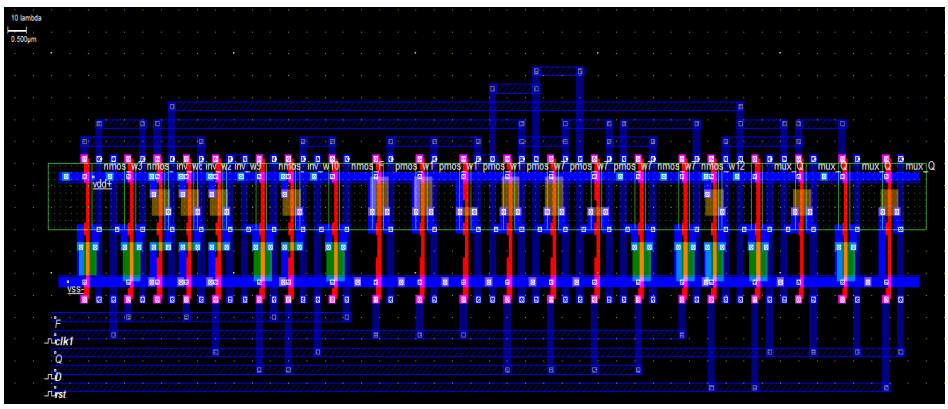

Figure 7. Layout of CGSAFF

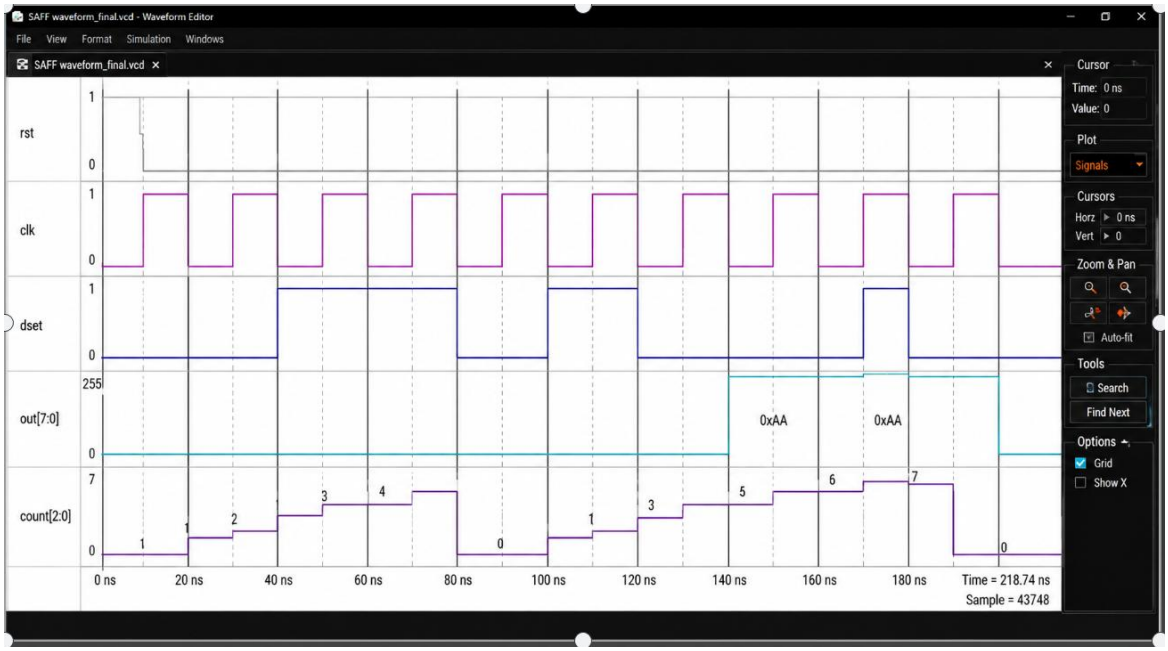

Figure 8. Simulation result of CGSAFF with power and delay analysis for 90 nm technology

Figure 9 shows the simulation result of CGSAFF with power and delay analysis for 65 nm technology. The Table 2 compares the performance of SAFF and CGSAFF using different CMOS technology nodes (90 nm and 65 nm). The parameters analyzed include power consumption, delay, step time, time scale, and clock voltage, which are important for evaluating the efficiency and speed of digital circuits.

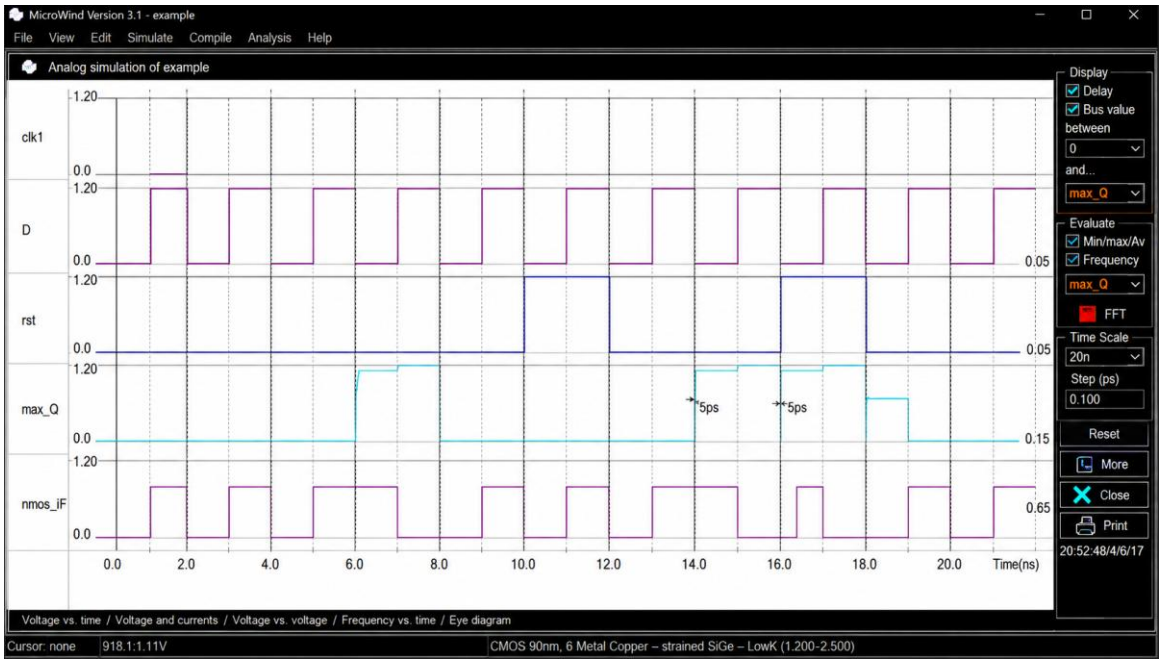

Figure 9. Simulation result of CGSAFF with power and delay analysis for 65 nm technology

The circuit was tested with different supply voltages depending on the technology node:

- 1.20 V and 2.50 V for 90 nm technology.
- 0.70 V and 2.50 V for 65 nm technology.

Table 2. Power and delay performance analysis

CMOS technology	Power (µW)	Step (ps)	Time scale (ns)	CGSAFF Lowk	Clk1	Delay in ps	Energy/ transition	Power/transistor (µW)
90 nm	22.42	0.100	20	1.20 V, 2.50 V	1.11 V	6	448480	0.801
65 nm	5.407	0.200	20	0.70 V, 2.50 V	0.77 V	7	108140	0.193
CMOS technology	Power (µW)	Delay ps	SAFF Energy transition	Power/transistor (µW)	-	-	-	-
90 nm	23.8	47	476000	0.915	-	-	-	-
65 nm	36.83	60	736600	1.416	-	-	-	-

From the Table 2, in 90 nm CMOS technology, the SAFF circuit consumes 0.238 µW power with a delay of 47 ps. In contrast, the CGSAFF circuit consumes 22.424 µW power with a step time of 0.100 ps and operates with a time scale of 20 ns. The operating voltages used are 1.20 V and 2.50 V, and the clock voltage is 1.11 V with a delay of 6 ps.

For 65 nm CMOS technology, the SAFF circuit shows 36.830 µW power consumption with a delay of 60 ps, while the CGSAFF circuit consumes 5.407 µW power with a step time of 0.200 ps and the same time scale of 20 ns. The operating voltages are 0.70 V and 2.50 V, and the clock voltage is 0.77 V with a delay of 7 ps. Overall, the comparison indicates that technology scaling (from 90 nm to 65 nm) affects both power consumption and delay characteristics. The results help in evaluating which FF design provides better power efficiency and performance for high-speed digital circuits and low-power VLSI applications. The RTL description of the proposed CBSAFF was synthesized using the Xilinx Vivado design suite (Version 2020.2) targeting the Xilinx Spartan-6 FPGA family (XC6SLX45-CSG324).

From Table 3, the suggested energy efficient architecture uses very few hardware resources according to the FPGA synthesis report suggesting a compact and area-efficient implementation. The entire design exhibits low logic complexity by using just two slice LUTs three slice registers and two occupied slices. While the SAFF module only needs one register and no extra LUT resources the CD module handles the majority of the combinational logic and uses two LUTs and two registers. Four Bonded I/O Blocks (IOBs) are used in the design for external signal interfacing and one BUFGCTRL is used for clock distribution. Additionally, the FPGAs efficient packing of logic and storage components is demonstrated by the use of just one LUT-Flip Flop pair. The suggested design is appropriate for energy-efficient and resource-constrained applications since it achieves low-area implementation with minimal FPGA overhead according to the overall resource utilization results.

Table 3. Hardware resource utilization summary of the proposed design

Name	Slice LUTs (20800)	Slice registers (41600)	Slice (8150)	LUT as logic (20800)	LUT flip flop pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Energy efficient FF	2	3	2	2	1	4	1
CD	2	2	1	2	1	0	0
SAFF	0	1	1	0	0	0	0

The proposed 8-bit energy-efficient SAFF architecture and its component modules the XOR AD and SAFF block are shown in the Table 4 along with their FPGA resource utilization. The synthesis results show that the entire design takes up very little FPGA resources indicating its hardware-efficient and compact implementation. The top-level module energy efficient SAFF 8-bit makes use of four occupied slices sixteen slice registers and five slice LUTs. Additionally, it uses only one BUFGCTRL for global clock distribution and 18 IOBs to interface the 8-bit input 8-bit output clock and reset signals. This low resource consumption attests to the design's suitability for low-power and area-constrained applications. The combinational logic operations in the design are handled by the XOR AD module. The fact that it uses three occupied slices eight slice registers and five slice LUTs shows that the majority of the logic resources are used to identify changes in the input data. By only producing an enable signal in response to a data transition the AD minimizes pointless switching activity. The SAFF modules straightforward and effective storage functionality is demonstrated by the fact that it only needs 8 slice registers and 2 occupied slices while using no LUT resources. Reduced dynamic power consumption results from the SAFF updating its output only when the AD is activated.

The suggested 8-bit low-power counter based on a SAFF uses FPGA resources as shown in Table 5. The design demonstrates a compact hardware implementation by using just 6 slice LUTs 8 slice registers and 3 slices. The suggested architectures area-efficient nature is confirmed by its effective use of LUT-FF pairs and low clocking resources which makes it appropriate for digital systems with limited power and resources.

Table 4. Hardware resource utilization summary of the proposed energy-efficient SAFF design

Name	Slice LUTs (20800)	Slice registers (41600)	Slice (8150)	LUT as rogic (20800)	Bonded IOB (106)	BUFGCTRL (32)
Energy efficient SAFF (8 bit)	5	16	4	5	18	1
AD (XOR)	5	8	3	5	0	0
SAFF (8-bit)	0	8	2	0	0	0

Table 5. Hardware resource utilization of the SAFF-based 8-bit low-power counter

Name	Slice LUTs (20800)	Slice registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT flip flop pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Low power 8-bit counter	6	8	3	6	5	10	1
SAFF (8-bit)	6	8	3	6	5	0	0

5. CONCLUSION

For digital and IoT systems a modified sense-amplifier-based FF has been introduced as a low-power option. The design aims to reduce energy consumption through an improved sensing stage and simulation results show that it performs better than the majority of current architectures in important metrics like average power dissipation layout area and PDP. To further increase overall energy efficiency the SAFF configuration incorporates clock-gating to prevent needless switching. The suggested FF functions steadily under a variety of operating conditions such as supply voltages between 0.5 V and 1.1 V and temperatures between –40 °C and 120 °C. Strong power savings are especially evident when input-toggle activity is high. It is advised to use the design down to 0. 34 V which guarantees robust behavior under aggressive voltage scaling for dependable operation and optimal performance. The proposed CGSAFF combines transistor-level optimization with an internal clock-gating mechanism to reduce needless switching activity, lower dynamic power and delay, and improve PDP while maintaining reliable operation under PVT variations, in contrast to conventional SAFFs that primarily improve speed and current clock-gating techniques that operate at the system level. The proposed flip-flop design can be further optimized by implementing post-layout analysis with full parasitic extraction and testing in advanced CMOS technology nodes to validate its practical efficiency. Experimental validation using prototype hardware or FPGA/ASIC implementation would also help confirm the real-time performance of the circuit. Furthermore, future studies may explore adaptive clock-gating techniques, improved transistor sizing, and integration with ultra-low-power IoT architectures to further reduce energy consumption and enhance overall system reliability. These improvements can make the proposed SAFF design more suitable for next-generation low-power digital and IoT applications.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST

Authors state no conflict of interest.

ETHICAL APPROVAL

No new human participants were recruited, and no additional experiments involving human subjects were conducted by the authors. Therefore, ethical approval and informed consent were not required for this study. All data were used in accordance with the dataset providers' terms and conditions.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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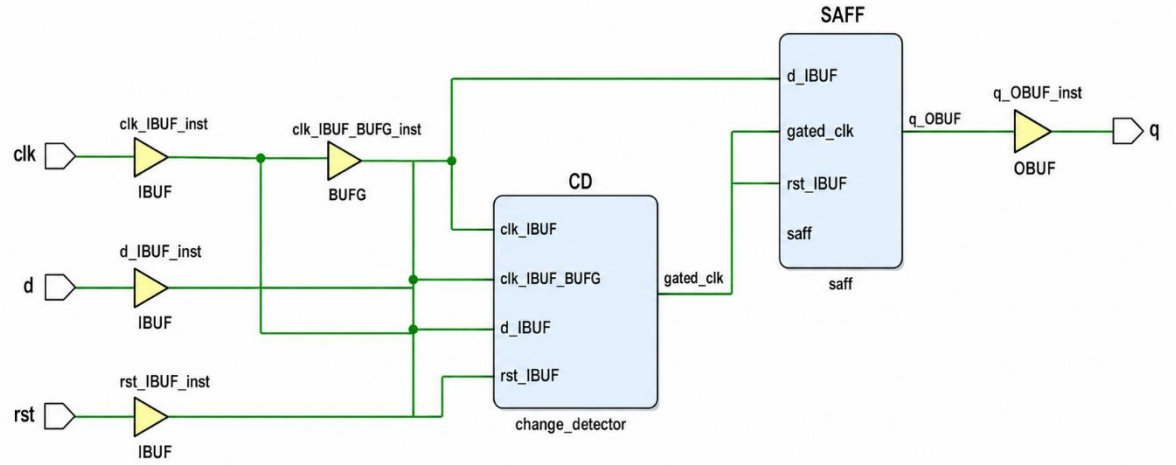
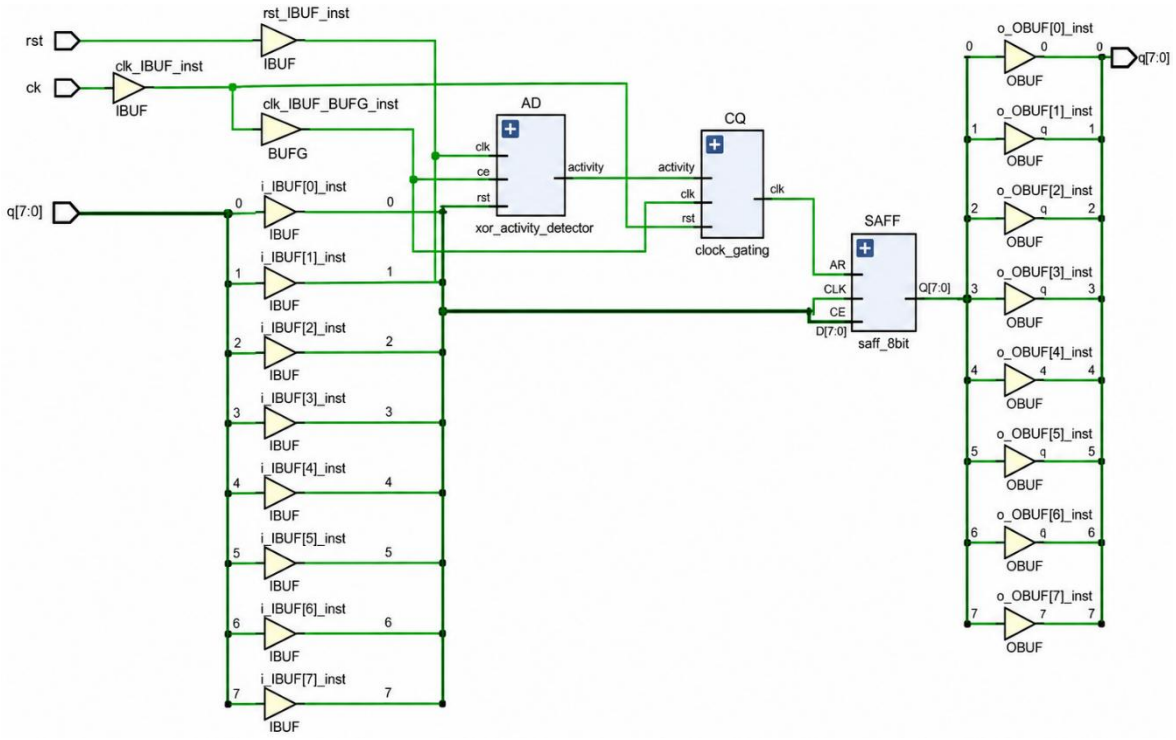
APPENDIX

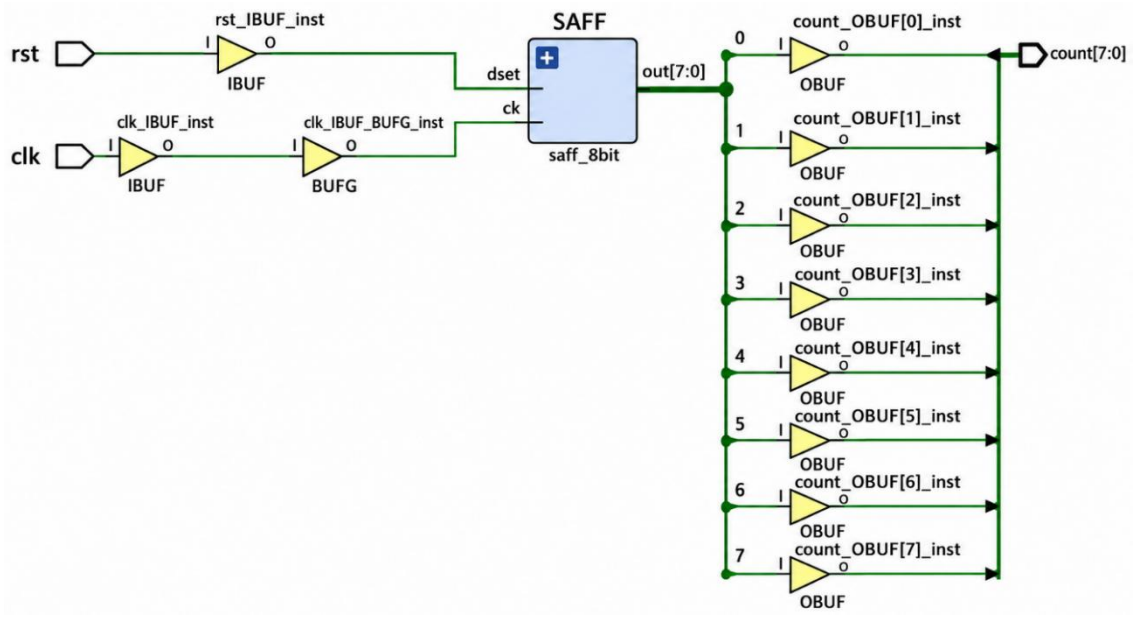


(a)



(b)

Figure 6. Schematic diagram of CGSAFF architecture and its application; (a) proposed and (b) proposed 8 bit CGSAFF



(c)

Figure 6. Schematic diagram of CGSAFF architecture and its application; (c) proposed 8 bit counter using CGSAFF *(continued)*

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