

Simulation study of memristor aided logic (MAGIC) based on CMOS NOR gate

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ABSTRACT

Memristor is a non-volatile new technology memory where the data stored as a resistance which the performance is influenced by the stateful logic design. Therefore, this study is an attempt to investigate the performance of the MAGIC NOR Gate stateful logic design using LTSPICE and targeted to 2 bits memory application. The objective is to investigate the performance of memristor based stateful logic design and schematics for memory application. Furthermore, the study been carried out by implementing the MAGIC NOR gate stateful logic schematic, then simulate the design in order to see the effects of performance including the electrical parameters compared to the others. Evidently, the improvement of MAGIC NOR gate contributes in reducing the number of NOR gate and CMOS count. Besides, the MAGIC NOR gates takes parallel inputs topology and eliminate the threshold voltage compared to IMPLY logic. Nevertheless, larger numbers of memristor required to stable the output consistency in MAGIC NOR gate schematic.

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1. INTRODUCTION

In recent years, renewed interest has been generated by the concept of a memristor which originally proposed by Leon Chua in 1971 [1–4]. Over the past few decades, the relentless migration of technology to the nanometer regime has resulted in high capacity storage and memory systems. Nonetheless, this aggressive scaling has a negative impact on the cost, performance and reliability of flash and DRAM technologies and architectures. Chua in [1, 5] suggested the memristor as an addition to the three well-known basic electronic components, a fourth fundamental component; resistor, capacitor and inductor. Basically, the Memristors and memristive devices are two terminal devices, where electrical current affects the device's resistance as shown in Figure 1.

As depicted in Figure 1, the device's resistance decreases when the current flows into the device (the upper arrow). The device's resistance increases when the current flows out of the device (the lower arrow). In addition, the memristors resistance is limited by a minimum R_{ON} resistance and a maximum R_{OFF} resistance. The terms memristor and memristive device are used interchangeably for simplicity in this brief as highlighted in [6, 7]. Furthermore, the concept of a memristor has been theoretical for nearly 40 years since

1971 [2]. The physical phenomenon of resistance switching in TiO_2 was connected to memristors by Hewlett Packard Laboratories in 2008 as reported in [8]. Several possible memristor applications have been submitted since 2008 after the discovery [4, 9-20].

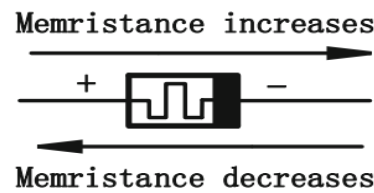


Figure 1. Symbol of the memristor. a thick black line represents the memristor's polarity

Furthermore, memristors also known as non-volatile new memory technologies and this includes resistive RAM (RRAM) and spin-transfer torque magnetoresistive RAM [3]. Memristor primary application is for memory as highlighted in [1, 2, 21] where data is stored by the resistance. Moreover, Memristor-based logic [2, 22, 23] is another interesting and new application of memristor. A stateful logic including the material involvement (IMPLY) is introduced in [2, 24, 25] as a memristor-based logic window. This approach does not require a complex structure and allows the gate function to be stable evaluated. Through applying a single voltage and two voltage pulse at the circuit gateway, a balanced evaluation is achieved. MAGIC NOR gate can also be produced in a crossbar, allowing memory computing. But, the MAGIC NOR gate and its performance is new topic which not discussed and highlighted in any study before. Therefore, this paper will focus on the design of MAGIC NOR gate schematic using LTSPICE and targeted to 2 bits memory application. Then, the objective of this project is to investigate the performance of this memristor based stateful logic design and schematics for further memory application.

2. OPERATING PRINCIPLE OF MEMRISTOR

Magic only include memristor within the gates of logic. The logical state of a MAGIC gate is represented as a resistance which the high and low resistance are respectively considered. Logical zero and one (the resistance of logical zero and logical one is known as R_{OFF} and R_{ON} for simplicity, respectively). The logic gates input and output are the logical states for the input and output of the memristor. The logic gates inputs and output are the logical memristor states. Unlike an IMPLY logic gate, the input and output require separate memristors. The MAGIC gates outputs are the initial state of the memristors input, and the output is the memristor's final logical state. In Figure 2 show that the both in_1 and in_2 are the gate inputs, and the final memristor output is the gate output.

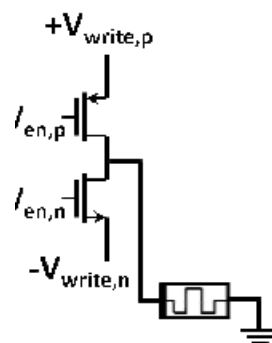


Figure 2. Example of placing a memristor in a stage of initialization

As shown in Figure 2, this is similar to write an analog circuit that can be configured. There are two sequential stages to operate a MAGIC gate. The first stage initializes a known logical state of the output memristor. A voltage V_0 is applied throughout the output memristors in the second stage of operation, depending on the logical state of the input and output memristors. The memristor's nonlinear properties, i.e. the threshold current or voltage are used to maintain proper operation. The voltage is adequate for different input combinations to adjust the logical state of the output memristor, i.e. the voltage/current memristor is

greater than the voltage/current threshold. While the output remains at the initialized state for other input combinations. The voltage/current memorizer is below the current or voltage limit. Note that for memristors with a threshold current, complete switching is not possible in some cases. It is possible to configure the memristors in several ways. Analog memristive circuits, as shown in Figure 2. As a regular write operation within the memory cells, MAGIC gates are achieved within memory initialization.

3. METHODOLOGY

Simulation of memristor connection with CMOS NOR gate is chosen in this study. The design was developed using LTSPICE based on the following steps or methodology summarize in Figure 3. As depicted in Figure 3, five phases of work involved in this study. First, in the review stage, several schematic and information related to the CMOS NOR gate and others memristor information are reviewed and analyzed. Based on the finding, the schematic of memristor connecting with the CMOS NOR gates were then drawn using LTSPICE. Then, the simulation between the CMOS NOR gate with memristor were carried out as to validate the design and getting the finding from the design. Followed by, the comparative between the propose design and IMPLY logic as to identify the pro and cons between both. The assessment between the CMOS NOR gate output result then carried out as in the final stage. This is to validate and summaries the overall finding from the study.

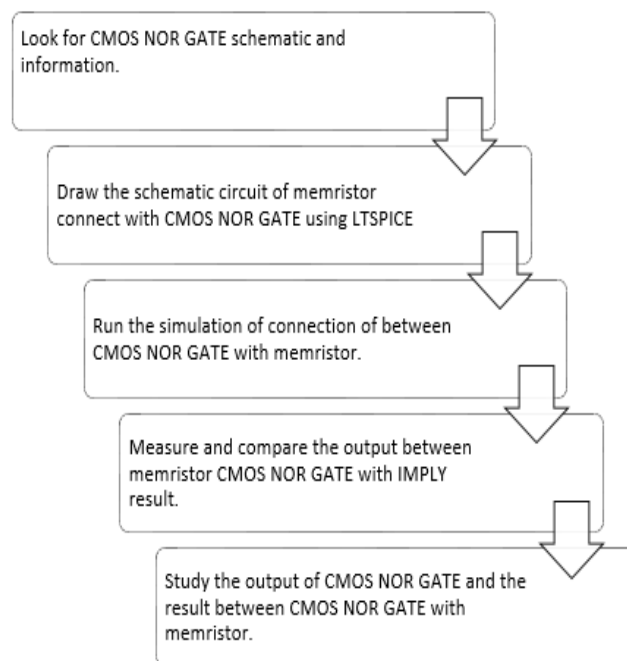


Figure 3. Flow of the MAGIC CMOS-NOR gate design

4. BASIC MEMRISTOR CIRCUIT

To the design the memristor circuit, the LTSPICE is used. The simple model of memristor is described in (1), As depicted in Figure 4, both of the x axis domain and the y axis range are bound between 0 and 1 for the simple model memristor. Therefore, the plot of integral function between 0 and 1 producing the plot as shown in Figure 5. As shown in Figure 5, the integral of the window function represent the state of x , between 0 and 1. This value is used to dynamically change a delta R value which delta R is $R_{off} - R_{on}$. As a result, a current source in series with a 1F capacitor and a resistor creates an integrator circuit, where the voltage on node x represents the integral.

$$f(x) = 1 - (2x - 1)^{2p} \quad (1)$$

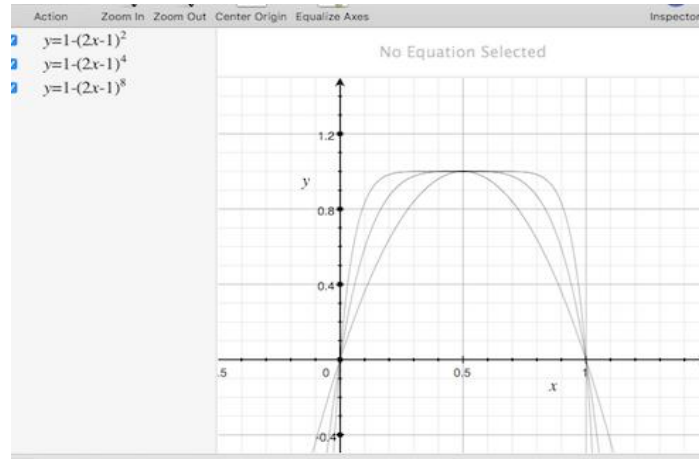


Figure 4. Simple model memristor circuit function

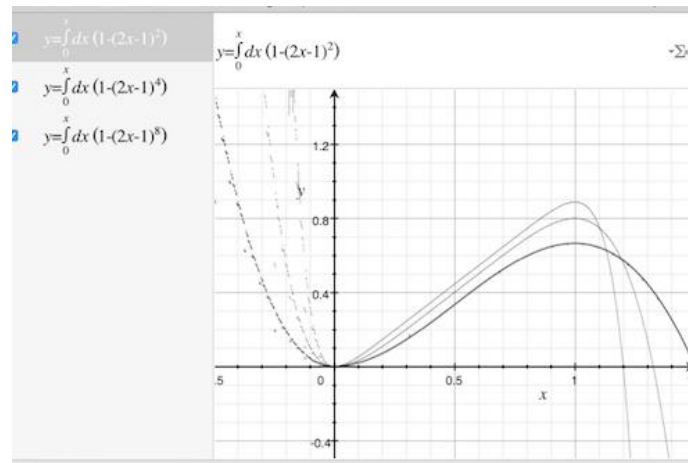


Figure 5. Plot of the integral function between 0 and 1

The symbol of memristor in LTSPICE is shown in Figure 6. From the memristor symbol, the node *A* refer as R_{off} and the node *B* refer as R_{on} . For the simple memristor circuit connection, V_{in} is set to sine with 1.2V with 1Hz oscillation. The voltage source is connected in series with memristor which the positive voltage source is connected to the memristor and the negative is connected to the ground as shown in Figure 7.

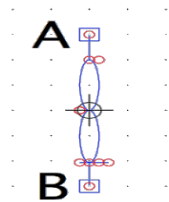


Figure 6. Symbol of memristor in LTSPICE

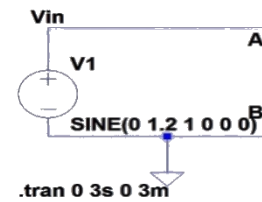


Figure 7. Memristor circuit

5. MEMRISTOR WITH NOR GATE

By using the CMOS method, the memristor NOR GATE circuit was constructed using two PMOS and two NMOS connected with three voltage supply. The first power supply is set at 5V and connected to the PMOS as an input while the rest are set as pulse input. Moreover, the first pulse input is set at 1V with $V_{on}=4V$, $delay=1s$, $T_{on}=1s$ and $period=2s$. On the other hand, the second pulse input is set at 0.95V with $V_{on}=4.05V$, $delay=0.5s$, $T_{on}=1s$ and $period=1s$. Three memristors were used in this circuit which one

memristor is connected at port A and B as an input and the other memristor connected to port F as an output as shown in Figure 8.

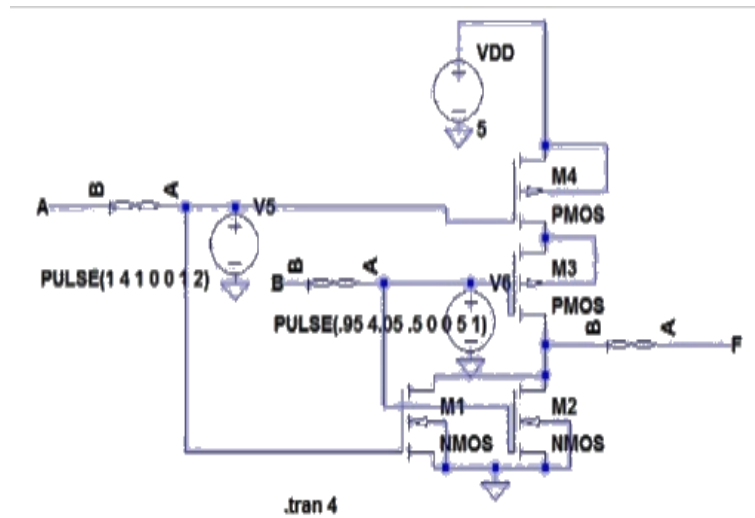


Figure 8. NOR CMOS circuit with 2 NMOS and 2 PMOS.

6. RESULT AND DISCUSSION

Based on the the memristor circuit in Figure 8, the simulation was performing with 3s interval for maximum time step of 3 minute. As to compy with the MAGIC NOR gate requirement, the logic gate's structure and connections are placed in a crossbar array, and the logic gate's logical state is represented as a resistance, as in a memristive memory. Based on the requirement, the result is generated for both LTSpice memristor hysteresis as shown in Figure 9 and the Current-Voltage characteristics of a linear ion drift TiO₂ memristor as shown in Figure 10.

On the other hand, stateful memristive logic gates can be integrated into a memristive crossbar array and these logic gates require an additional resistor in each crossbar array row. In addition, the IMPLY operation is not logically complete, unlike the NOR gate operation, and requires the FALSE operation (writing a logical zero to a memristor). A comparison between memristive IMPLY and memristor with NOR GATE is listed in Table 1.

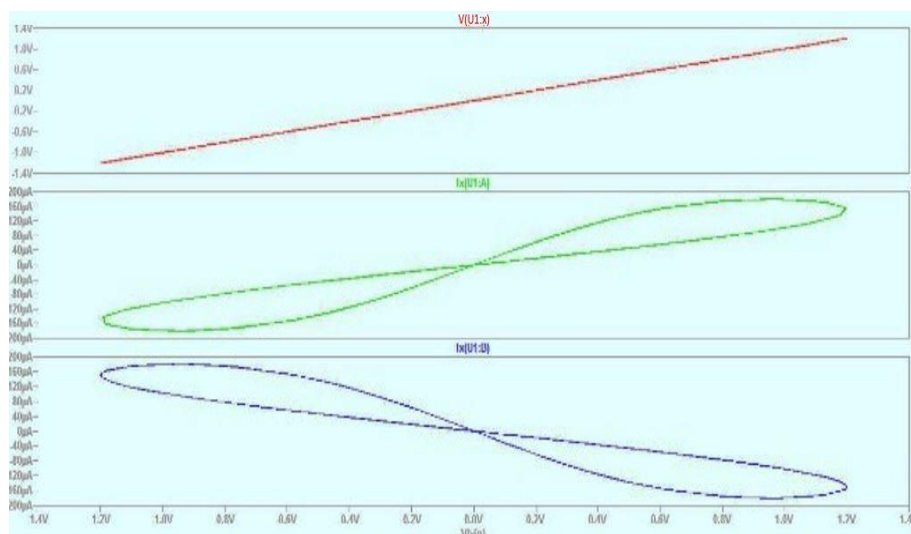


Figure 9. Memristor hysteresis result

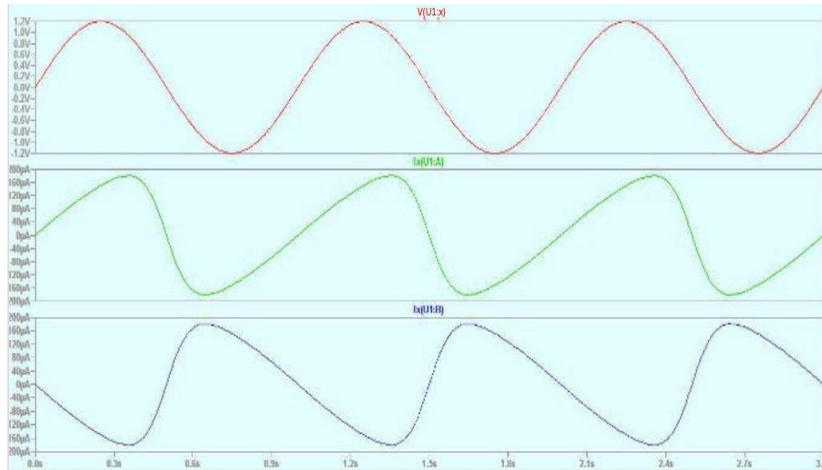


Figure 10. Memristor current-voltage result

Table 1. Comparison between IMPLY and MAGIC

	IMPLY [25]	MEMRISTOR WITH NOR GATE
No. of Voltage	2	3
Separate input and output	No	Yes
Basic Function	IMPLY (+FALSE)	NOR
No. of memristor for NOR	3(+ a resistor)	3
No. of clock cycles for NOR	4	2
Within memory	Yes	Yes
Logically complete	Requires FALSE	Yes

As highlighted in Table 1, the NOR gate is more stable as compare to the IMPLY logic. But, the NOR gate required more power supply as compare to IMPLY logic. Additional resistor make IMPLY more complex as compare to the NOR gate. Moreover, the LTSPICE simulations of a two-input MAGIC NOR gate using 2 CMOS is shown in Figure 11. As shown in Figure 11, the output of the simulation prove the logic function of NOR gate truth table. Moreover, the NOR gate not only comply with the memristor memory design but NOR gate logic as well.

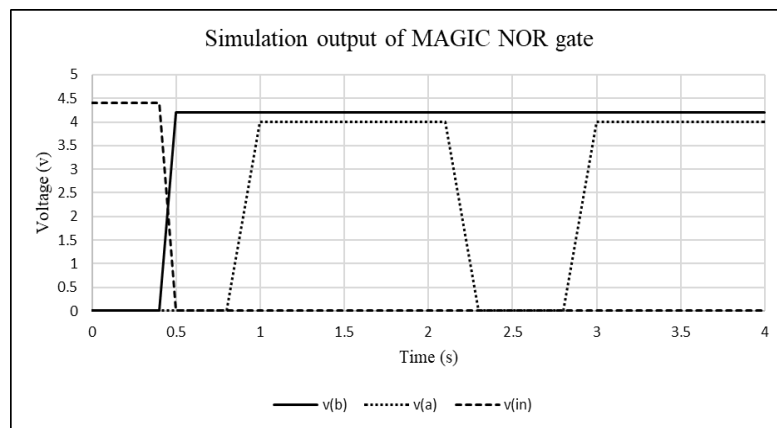


Figure 11. The simulation output of MAGIC NOR gate

7. CONCLUSION

As the consequences, memristor memory design has always demanded the optimum performance in terms of logic stability, sizing and gate count. This study found that the NOR Gate design improve the logic stability, reduce the memristor count and eliminate threshold voltage but need large schematic design and required additional power source. Furthermore, the NOR Gate is able to reduce the complexity in the circuit by separating the inputs and output. Nevertheless, the number of clock cycle is reducing as compared to the others.

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