

A 9T FinFET SRAM cell for ultra-low power application in the subthreshold regime

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ABSTRACT

Due to the scaling of the CMOS, the limitations of these devices raised the need for alternative nano-devices. Various devices are proposed like FinFET, TFET, CNTFET. Among these, the FinFET emerges as one of the promising devices which can replace the CMOS due to its low leakage in the nanometer regime. The electronics devices are nowadays more compact and efficient in terms of battery consumption. The CMOS SRAMs have been replaced by the FinFET SRAMs due to the scaling limitations of the CMOS. Two FinFET SRAM cells have been which power efficient are and having high stability. Performance comparison of these cells has been done to analyze the leakage power and the static noise margins. The simulation of the cells is done at 20 nm FinFET technology. It has been analyzed that the write margin of improved 9T SRAM cell achieves an improvement of 1.49x. The read margin is also showing a drastic improvement over the existing cells which has been compared in the paper. The hold margin was found to be better in the case of the proposed SRAM cell at 0.4 V. The gate length has been varied to find the effect on read margin with gate length.

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1. INTRODUCTION

Miniaturization has become the trend for electronic gadgets. The market trend is towards handy portable and compact devices. Almost all the electronics devices have the involvement of CMOS and scaling of the CMOS has made the miniaturization dream possible. All smart gadgets are nowadays coming in small compact sizes. These devices have various circuits but the one which is common to all is processor and memory. When we think of a handheld device at the same time, we can realize that the memory size would also be reduced. The speed of the devices should also be fast, so memories like SRAM started gaining popularity.

Scaling of the sizes is possible because of the reduction of the size of CMOS, this size reduction has come up with certain issues like power and stability of the devices. Both the issues of power and stability are important performance matrix of the SRAM Memories. Several issues like high power consumption, leakage current, stability, process variations. have been raised and addressed by the researchers. The reduction in the supply voltage which is necessary due to the scaling of the device size also resulted in the reduction of the threshold voltage of the CMOS devices which was one of the major concerns. So many solutions have been proposed among them the subthreshold operation [1] was one of the solutions, where the device works below

the threshold voltage, but it affected the 6T SRAM stability issues. To address the limitations the conventional 6T SRAM cell was then replaced by other versions of SRAM cells like 7T, 8T, 9T, 10T SRAM cells for enhancing stability criteria and reduce the power.

2. LITERATURE REVIEW

CMOS scaling has now come to a limit and alternate solutions for silicon or CMOS devices have come up like TFET, FinFETs, CNTs. FinFET device seems to be a promising device and can be one of the most promising candidates for low power emerging electronics circuits. FinFETs can work at low medium frequency operations at lower voltages. FinFET has higher threshold voltages and it has overcome the short channel effect of CMOS, so this can be another good choice for SRAM memories [2], [3]. Memories using FinFET has been proposed and accepted largely due to the benefit of small size and low leakage over CMOS. After Intel's recent announcement that FinFET will be its basic CMOS device beginning at the 22 nm node, the development of nanoscale FinFET has increased [4]. The number of gates in FinFET can be two, or even three. The quasi-planar structure, and the uncommon processing thereby implied, can thus be effectively traded off. FinFETs are being fabricated on the bulk and silicon on insulator (SOI) wafers. In bulk FinFETs, all fins used a common Si substrate while in SOI fins which are physically isolated.

Based on the gates FinFETs can be classified as shorted gate and independent gate FinFETs. A FinFET whose gates are independently controlled is described as an independent-gate (IG) FinFET, whereas in shorted gate as the name depicts both the gates of the FinFET are being shorted. Tied gate FinFET is the other name of the SG FinFET. Threshold voltage can be modulated by biasing the gates of IG FinFET which can be useful for reducing the leakage power. SG FinFETs are the fastest as they provide better control of the channel and improved drive strength [5], [6].

To enhance the stability and reduce the power various SRAMs have been proposed from time to time by researchers. SRAM has been classified as single port & dual port (multiport), symmetric & asymmetric SRAMs. A novel 9T SRM cell using CMOS has been proposed in [7]. Pal and Islam [8] 8T SRAM has been proposed for enhanced stability and low leakage. Some FinFET SRAMs have also been proposed for improvements in terms of stability and leakage. Gupta *et al.* [9] author proposed SRAM with pass gate feedback. To increase robustness in FinFET SRAM author has used pass p-type access transistor [10]. 8T FinFET SRAM cell has been proposed with improved read and write margins in [11]. Birla [12] subthreshold FinFET SRAM has been proposed for low power applications. Robust 6T FinFET SRAM cell has been studied in [13]. In this work a 9T SRAM using FinFET has been compared with 9T improved FinFET SRAM in which 9 transistors have been used to improve the leakage and the stability of the cell. The 10T SRAM FinFET SRAM is proposed with high stability and read margin [14]. Feedback mechanism using Schmitt trigger-based SRAMs are proposed in [15], [16]. Dual port SRAM for improved stability has been proposed in [17]. FinFET SRAM with minimum variations and improved stability has been proposed in [18]. FinFET SRM with asymmetrical bitlines has been proposed in [19].

3. PROPOSED WORK

In this paper, an SRAM cell consisting of nine FinFET transistors has been proposed. Due to the limitation of the scaling down of CMOS device FinFET has been used to improve the overall performance which includes efficiency, power, and area. Various FinFET SRAM cells have been proposed by the designers which are low leakage and having improved static noise margins. These cells are proposed for an improvement in the leakage current and stability of the cell.

Figure 1 shows a conventional 6T transistor using FinFET. Here, two-bit lines: One is named as BL and the other as BLB is used. The one-word line named WL is also used to evaluate the working of the FinFET SRAM cell. The structure of the cells looks like a basic 6T cell, the only thing with 3 extra transistors. The main problem with the conventional 6T transistors as read disturb. However, due to device scaling, voltage is scaled down which results in decreased noise margins. This lowers the stability of the 6T SRAM cell. Figure 2 and Figure 3 shows the two proposed cells namely, 9T FinFET SRAM and 9T improved FinFET SRAM, the cells have a structure similar to 8T SRAM with one extra transistor deployed to enhance the performance of the cell.

3.1. 9T FinFET SRAM cell

Figure 2 shows the projected 9T SRAM cell using FinFET consisting of nine N-type FinFET transistors. The extra transistors used in this circuit from the conventional circuit helps in reducing the leakage current and the SRAM removes the limitation of the single port SRAM cell as it is a dual-port SRAM cell. The write operation is performed when the word line (WL) is kept at a high voltage which turns the access FinFET transistors of the cell ON. Since transistor M9 is connected to WL which is high so M9 will also be

high. Q and QB are the storage nodes assuming that initially Q stores logic 1 and QB will store logic 0. To write logic 0 at node Q we need to keep BL at logic 0 and BLB at Vdd. Node Q will discharge through M5 by BL and voltage at node QB starts increasing toward Vdd through M6 by BLB. Voltage stored at node Q will start discharging through M7 to the ground. While node QB starts charging as BLB is kept at Vdd through the access transistor. Node Q has the other two paths to discharge through M4 and M9 and also through M8. So data is written successfully. Similarly, for writing logic 1 at Q and QB at logic 0 keep the BL at Vdd and BLB at logic 0.

While reading, i.e., the read operation, bit-lines (BL and BLB) are precharged to Vdd and then keeping the WL to Vdd. Transistor M9 will be ON during the read and write operation. If node Q is at logic 1, transistor M4 will be ON and access transistor M5 will be ON. BL will be discharged through M5 and either through path M4 and M9 or M8 and ground. Similarly, if Q is at 0, BL will be discharged through M5 which is ON followed by M7 and ground. So, depending on the content of the storage nodes M3/M4 and M7/M8 will be ON and helps in discharging the BL. Hold operation is done by lowering the word line to GND as done in conventional 6T transistors. If WL will be assigned logic 0 the extra transistor M9 will also be Off, helping in reducing the leakage power.

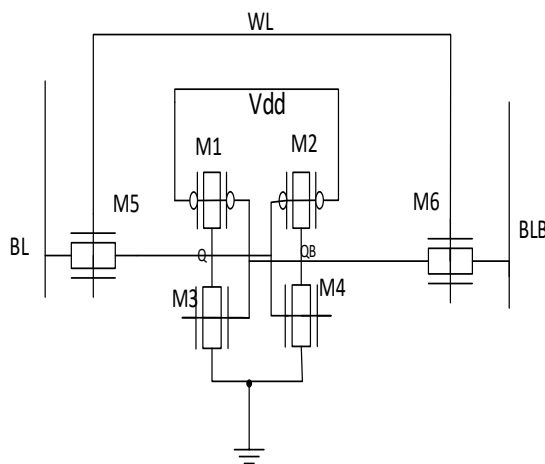


Figure 1. Conventional 6T SRAM FinFET cell

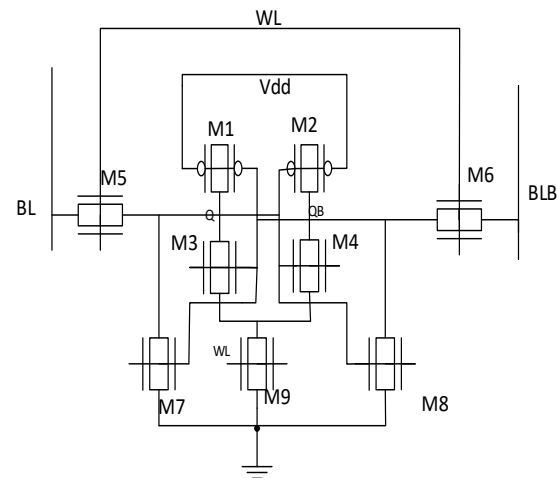


Figure 2. 9T SRAM FinFET cell

3.2. 9T FinFET improved SRAM cell

The improved version of the proposed 9T SRAM cell is similar in structure and working as to the 9T SRAM using FinFET. The improved version uses an extra transistor used is PMOS. This PMOS is being utilized in place of the NMOS in the 9T SRAM cell. Here, the extra transistor is PMOS which is controlled by a Cnt signal. The WL should be high, the bit lines are high according to the data which is to be written into the memory cell, Let's assume that the data to be written is logic 1, in this case, the BL should be kept at high voltage and BLB should be at low voltage. The only difference in this proposed cell is that here we have a control signal (Cnt) which remains logic "0" during read and write operations. This in turn on the PMOS which helps in reducing leakage current. The working of the cell is similar to the 9T FinFET SRAM cell as discussed in section 2.

4. PERFORMANCE ANALYSIS OF THE CELL

Various performance parameters of the cells are being considered in this paper like leakage current, stability parameters which include the read, write, and hold margin along with the effect of variation of the gate length on the stability. The cell proposed in Figure 2 and Figure 3 has been simulated using FinFET 20nm technology. The cells have been proposed for subthreshold conduction and the supply voltage has range has been kept in the range of 0.1V to 0.4V. In this paper, the leakage current has been analyzed and calculated along with the stability of the cell with read margin, write margin & hold margin have been determined and compared using the conventional SRAM cells. The simulation has been done using HSPICE at 20nm FinFET technology.

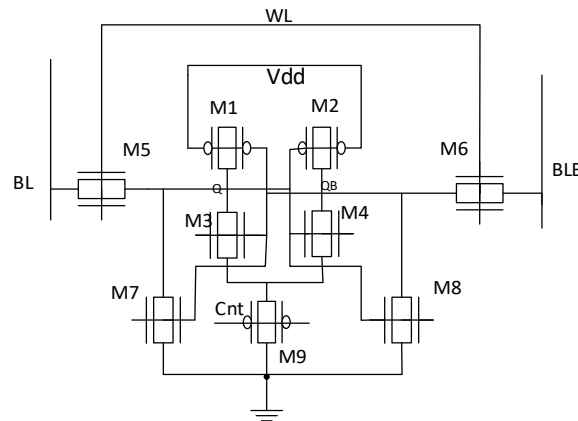


Figure 3. 9T FinFET improved SRAM cell

4.1. Leakage power dissipation

Leakage power dissipation is one of the key concern areas in handheld devices and all the handheld devices consist of SRAMs, so it will be a major concern for the memories like SRAM. Leakage current is measured majorly when memory remains idle, in cache memory leakage power is of major concern to focus on. The static power dissipation is calculated for both the proposed cells. The Static Power Dissipation for the proposed 9T SRAM cell is 1.5nW and for 9T FinFET, the improved SRAM cell was 1.1nW which was an improvement of 1.36x. Figure 4 shows the leakage current of the 9T SRAM and 9T improved SRAM cell at a subthreshold voltage of 0.4V. The leakage current measured is 77nA for 9T FinFET SRAM Cell and 69nA of the proposed FinFET SRAM Table.

4.2. Stability factors

Static Noise Margin SNM is the key parameter in accessing the stability of the cell. It can be determined using the butterfly curve or N curves [20], [21]. There are three types of stability parameters used to find for an SRAM cell: read margin (RM), write margin (WM) & hold margin (HM).

4.2.1. Write margin

The potential difference of the two-bit line levels which is responsible for flipping the data is defined as WM. The write-ability of the SRAM cell is evaluated by WM [22]. Figure 5 shows the WM for the three FinFET SRAM cells. It has been observed that the 9T improved SRAM FinFET cell has a better WM than the conventional 6T SRAM cell and proposed 9T SRAM cells. The write margin for the proposed 9T SRAM cell is 177.4V and for the 9T improved SRAM cell has 264mV at 0.4V. The improved 9T SRAM cell shows an improvement of 1.49x over 9T SRAM at subthreshold voltage.

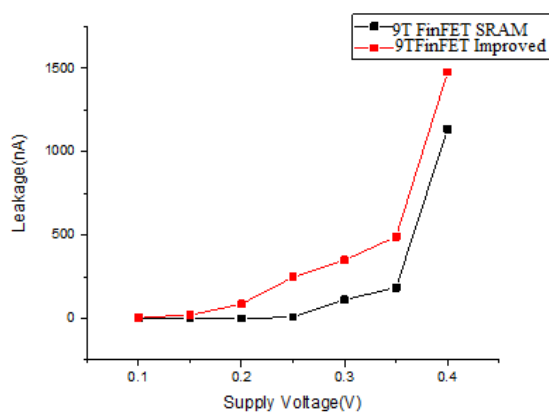


Figure 4. Leakage current of the various SRAM cells

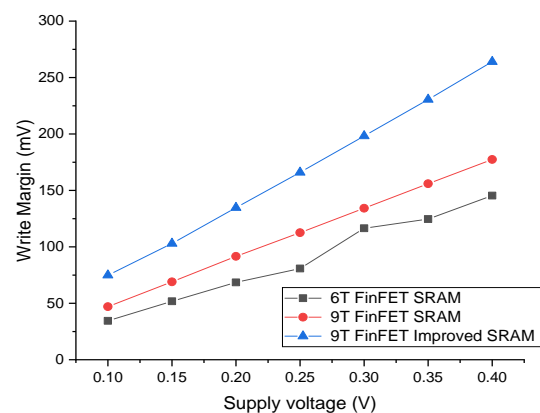


Figure 5. Write the margin of the various SRAM cells

4.2.2. Read margin

Read margin is used to determine the read stability. SRAM cells are most affected by noise during read operation only as read failure is a common issue in most of the SRAM cells. The read stability for an SRAM cell can be determined by RM. During a read operation, a voltage divider is formed between the access transistor and pull-down transistor and so, the node which was at 0V has raised to some positive voltage. A small voltage can change the stored value so RSNM is very much prone to noise and thus important [23]. Seevinck *et al.* [24] the noise margin is calculated using the butterfly curve in which it is said that the side length of the biggest square which can be embedded in the two lobes of the curve determines the SNM.

Figure 6 shows the variation of RM of 6T SRAM, 9T SRAM & 9T improved SRAM cell. The RM for the 9T improved SRAM cell is 170mV and for the 9T SRAM cell is 125mV at 0.4V. At 0.4V supply voltage, 9T improved SRAM cell has 1.36x times read margin than 9T SRAM cell. The 9T improved SRAM cell proves to be better in read operation also.

4.2.3. Hold margin

A cell in its idle state is considered to hold the data, Hold SNM is a metric used to measure how well the cell has held the data. Hold SNM is decreased if the supply voltage is reduced, "Data retention voltage (DRV) is the minimum voltage at which the cell can continue to hold its state" [25].

The hold stability in terms of the HM in the subthreshold operations has been calculated for the SRAM cell for three cells 6T, 9T SRAM cell, and 9T improved SRAM cell as shown in Figure 7 and it can be noticed that 9T improved SRAM cell has better hold the margin as compared to the other two cells. AT 0.4 V the hold margin of the 9T FinFET SRAM cell is 264mV while for the 9T FinFET cell is 177.5mV and for the 6T SRAM cell, it is 144mV. There is an improvement in the hold margin by 1.25X from the conventional 6T SRAM cell.

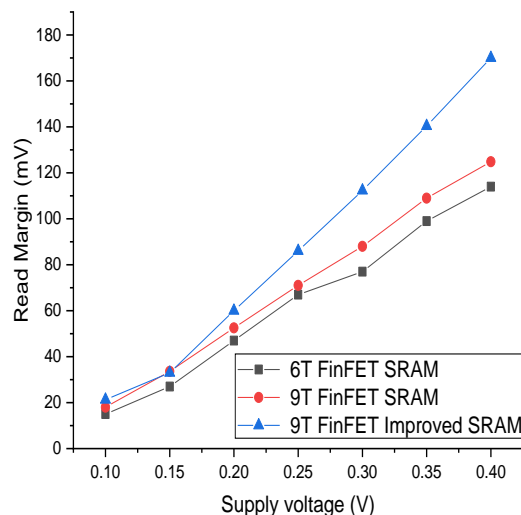


Figure 6. Read margin of the various SRAM cells

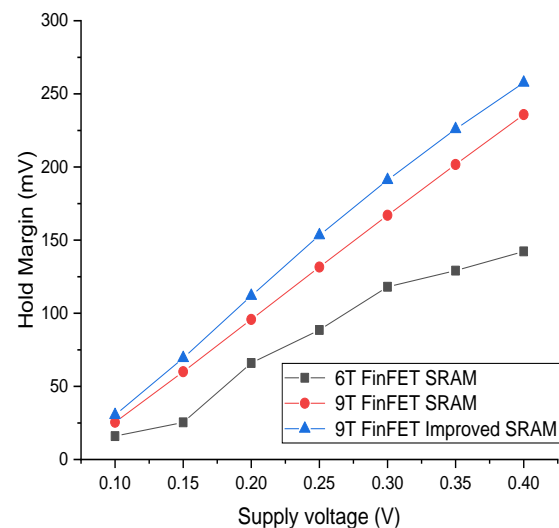


Figure 7. Hold margin of the various SRAM cells

4.3. Effect of gate length over the RM

The previous section discussed the stability factors concerning the variation of the supply voltage. Effect of stability factors i.e. RM, WM, and HM by varying the gate length has been found for 9T SRAM cell & 9T improved SRAM cell. The effect of variation of gate length on WSNM & gate length was negligible in both the cells and the effect on RSNM is considerable as shown in Figure 8. RSNM of the gate can be increased up to 20% if gate length is increased by 10% in 9T improved SRAM cell. The variation in RSNM is more in 9T improved SRAM cell as compared to a 9T SRAM cell.

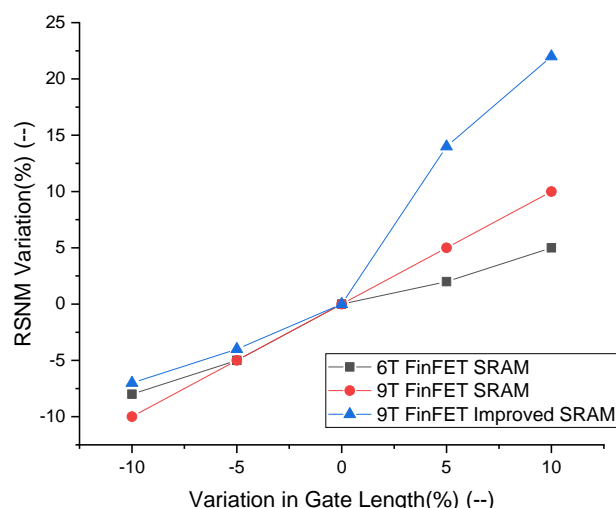


Figure 8. RSNM variation wrt. to gate length

5. CONCLUSION

In this paper, two different SRAM cells have been projected using FinFET for better stability and less leakage current. The leakage power and stability are found better in a 9T improved SRM cell as compared to a 9T SRAM cell. Both the cells have shown better overall better performance from 6T SRAM cells. Hold margin improved by 1.2x, read margin improved by 1.36x, and write margin improved by 1.49x. The effect of variation of gate length has also been found and seen that increasing the gate length will increase the RSNM. The future scope of this work is an SRAM array that can be designed and simulated for various operations. The speed can be optimized which is the future scope of this work. The only limitation of 9T improved SRAM cell is that since one extra PMOS transistor is used it can increase the area.

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