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Design and implementation of pulse width modulation gate control signals for two-level three-phase inverters

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ABSTRACT

The switching control circuit in a DC to AC inverter is the critical part that is applied to control the power transistors insulated-gate bipolar transistor (IGBTs) and metal-oxide semiconductor field-effect transistor (MOSFETs). This paper proposes a high-performance and low-cost pulse width modulation (PWM) control signal with a 120º phase shift circuit for a two-level three-phase inverter. Typically, a PWM signal with a 120º phase shift for three-phase inverters is generated with the help of analogue components with more complicated designs and power losses or by using a microcontroller with necessary programming or coding. The proposed solution is to design a 120° three-phase shift circuit based on D flip-flops and the 555-timer to generate the clock signal for the flip-flop input in addition to the dead-time control circuit. The proposed circuit is controlled by one square wave signal as an input signal to generate six output PWM control signals at 50 Hz to operate six MOSFETs in the three-phase inverter. Simulation results in power simulation software PSIM and PROTEUS simulation tools are used to verify the proposed circuit. Hardware implementation of the proposed circuit and three-phase inverter is carried out to validate the performance of the proposed design.

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1. INTRODUCTION

Recently, with the continuous revolution of using solar photovoltaic (PV) energy, power-generating techniques are becoming increasingly relevant with the push toward environmentally friendly and naturally occurring energy sources benevolent methods. Because of the rapid development in the production of electronic semiconductors, the high-performance design of power inverters has faced several challenges [1]–[3]. The conventional two-level, three-phase voltage source inverter (VSI), used in numerous applications including electrical motors, electric vehicles (EVs), and wind turbine systems, is thought to be the most widely used converter architecture [4]. Inverter is an electronic device which contains various power switches. By applying proper control pulses to these switches, AC power can be generated from DC input [5]–[8].

One of the major problems that the designers must deal with is how to adjust the voltage of the gate driver for the power switches while maintaining high safety isolation. These challenges are to design reliable PWM gate drivers that are suitable and ensure quick ON/OFF transitions for operations. Several forms of control driver circuits are employed to generate control signals for power converters [9]. A high switching

frequency is presented in [10] to operate the power switches of the three-phase inverter, which is used to improve the performance of the total harmonic distortion (THD) according to the alternative switching approach. Pulse width modulation (PWM) signals are often produced by digital control circuits, although they can also be produced by analog control circuits and programmable microcontrollers. However, digital control techniques can provide excellent flexibility with low-tech hardware components and a higher switching frequency. The analog PWM method necessitates many passive components, increasing power consumption and decreasing stability [11]. Active driver circuits using analogue circuits such as diodes and transistors have been proposed [12], [13]. However, it is not able to realize high-speed control signals due to component delay time. A programmable gate control circuit utilizes full digital control to solve the active gate driver circuit drawback [14]–[16]. To drive the power switches, a bootstrap driver circuit is commonly used; however, it is unreliable, with any faults occurring when the controller part is not isolated [17], [18]. Selecting a suitable modulation technique for the inverter design is the most important step toward realizing a low THD in the output voltage waveform. Several types of PWM generation schemes can be applied for gate controller circuit of the inverters, such as the standard PWM, Sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), and the selective harmonic elimination pulse width modulation (SHEPWM) method [19]–[21]. A pulse width modulation has been generated using the multicarrier sinusoidal pulse width modulation method to operate a 15-level multilevel inverter presented in [22]. The enhanced digital space vector pulse width modulation could create clocks by employing a digital clock manager and phase-locked loop (PLL). The modified digital space vector modulation is produced on a low-cost field programmable gate array (FPGA) for three-phase inverters [23]. A single-phase full-bridge inverter is designed based on the selective harmonic elimination method. An Arduino Mega has been used to determine the switching angles of the control signal and produce the PWM [24]. A three-phase full-bridge inverter is the main device utilized to derive induction motor and AC supplies. The output phase shift of the three-phase inverters is mutually phase-shifted by a 120-degree angle [25]. Three-phase shift signals with a 120-degree have been generated using a programmable microcontroller [26]. An analogue circuit based on operational amplifiers has been proposed to produce a three-stage phase shift with a 120-degree [27].

To implement a higher performance, low-cost gate controller circuit, this paper proposes a new 50 Hz single-input multi-output PWM gate controller circuit for three-phase inverters based on D flip-flops and the 555-timer. A 555 timer is applied to generate square wave PWM with a 50% duty cycle as an input to the control gate circuit. Three-phase shift signals based on digital flip-flops with a dead-time control and gate driver circuit have been proposed to operate the six power switches of the two-level three-phase inverter. Simulation results and prototype circuits have been utilized to validate the performance of the proposed design.

2. THREE-PHASE INVERTER

In industrial applications, three-phase inverters are more widely applied to drive induction motors and other three-phase AC equipment. The two-level three-phase inverter circuit consists of six power switches as insulated-gate bipolar transistor (IGBTs) or metal-oxide semiconductor field-effect transistor (MOSFETs) as shown in Figure 1. Each phase has two switches controlled by a PWM signal. To prevent a short circuit, the switches in the same phase are not turned on at the same time. Two methods are used to control the inverter switches: 120° conduction mode and 180° conduction mode. In this paper, the 180° conduction mode has been used to design the proposed control circuit. The switch timing occurs every 60° as shown in Figure 2. Where Figure 2(a) shows the switches timing occurs every 60° and Figure 2(b) shows the phase voltage of the three-phase inverter in 180° conduction mode.

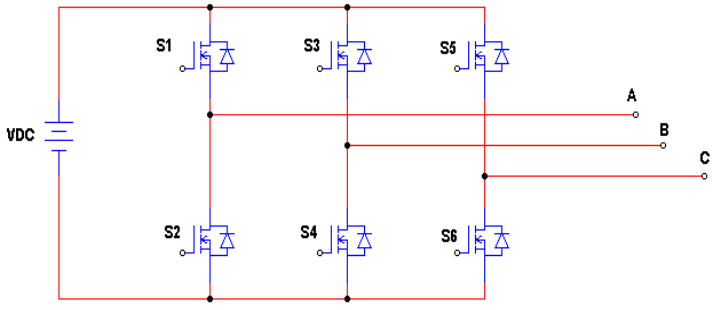
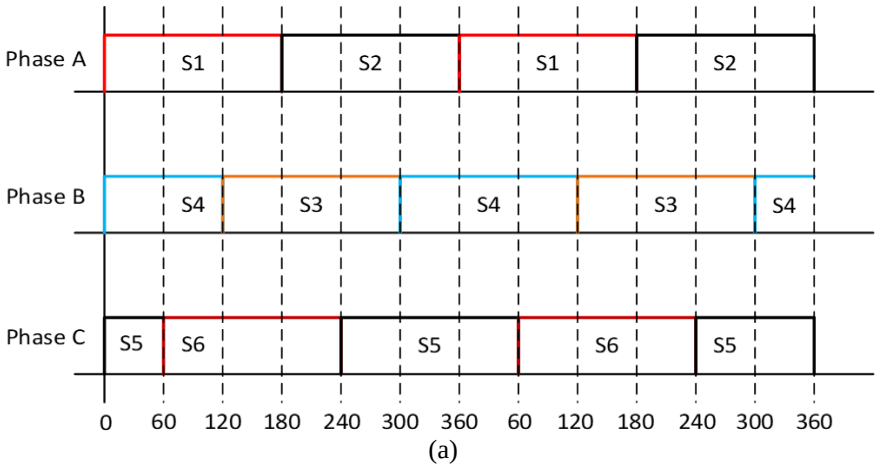
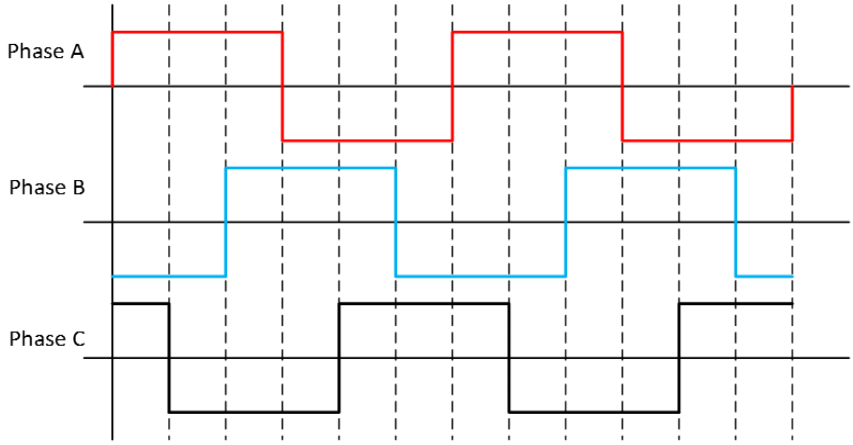


Figure 1. Two-level three-phase inverter circuit diagram



(a)



(b)

Figure 2. Control signals for switches; (a) the switches timing occurs every 60° and (b) the phase voltage of the three-phase inverter in 180º conduction mode

3. PROPOSED PWM CONTROL CIRCUIT

A high-performance, low-cost PWM gate control circuit for three-phase inverters to control six power switches with 120º phase-shift and dead-time generation circuit is proposed in this study. The block diagram of the proposed design is shown in Figure 3. The circuit is divided into four stages: square wave generator with 50% duty cycle, three-phase PWM control circuit with 120º phase shift, dead-time control circuit, and the driver circuit.

3.1. Square wave generator module

In this section, 50% duty cycle square wave PWM signal is produced by a 555-timer IC. As the clock signal to the next stage, a multi-PWM control circuit with a 120º phase shift oscillator. An astable multivibrator circuit based on the 555-timer is low cost and simple to implement using a few capacitors and resistors [28]. The values of the resistors and capacitors affect the frequency and duty cycle of the generated signal. The period time (T), frequency (f), and duty cycle (D) are determined by (1) to (3):

$$T = 0.693(R_1 + R_2)C \quad (1)$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1+2R_2)C} \quad (2)$$

$$D = \left(\frac{R_1+R_2}{R_1+2R_2}\right) \times 100 \quad (3)$$

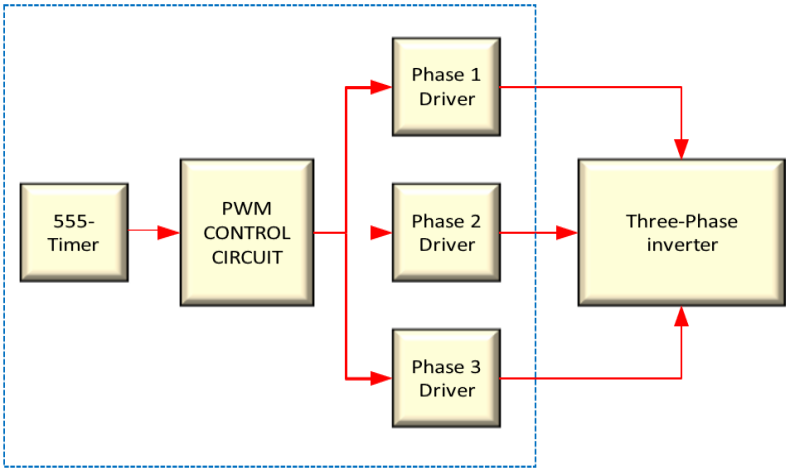


Figure 3. The block diagram of the proposed PWM module

3.2. A 120-degree three-phase shift circuit

A PWM control circuit based on a D flip-flop is proposed to provide switching control signals with 120º phase shift for three-phase inverter power transistors. The D flip-flop is the main part that is used to generate 50 Hz PWM signals with a 120º phase shift. The number of D flip-flops required to design the circuit is based on the number of high-side transistors of the inverter. Therefore, three D flip-flops are used in this design. The switching diagram of the two-level three-phase inverter in Figure 4 is used to design the control circuit. Because of the complementary status of the two switches in the same inverter leg, only the signal of the upper switches (S1, S3, and S5) in each phase is used for designing the circuit. The state diagram of the inverter switching operation is determined from the switching diagram as presented in Figure 5. Each state in the diagram represents the status of the switching in all phases of the inverter. At the switching period, the initial state (000) occurs when all switches are OFF. When S1 is ON, S2 is OFF, and S3 is ON, the state is changed to the following example (101). When S1 is ON while S2 and S3 are OFF, the next state (100) is reached. When S1 is ON, S2 is ON, and S3 is OFF, the subsequent transfer (110) takes place. When S1 is OFF, S2 is ON, and S3 is OFF, the state (010) is reached. The switches S1 is OFF, S2 and S3 are ON, and the state (011) occurs. However, the last transfer (001) occurred when S1 was turned off, S2 was turned off, and S3 was turned on. In the next switching period, all states will repeat themselves.

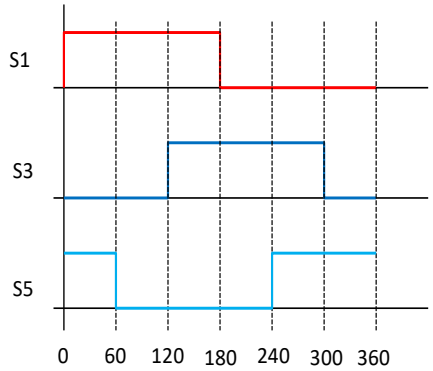


Figure 4. Three phase inverter switching diagram

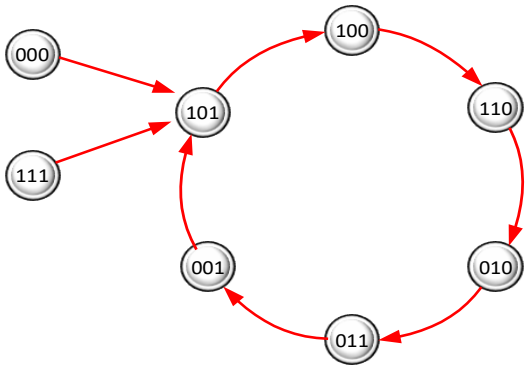


Figure 5. The state diagram of the inverter switching status

The following step is to determine the state table of the present switching states and the following switching states based on the state diagram as shown in Table 1. Each state of the switches (S1, S3, and S5) has a separate Boolean function. Karnaugh map is used to determine the Boolean functions for each switch depending on the D flip-flop state.

a. Karnaugh map and Boolean function of the first phase D flip-flop

Q3 \ Q1.Q2	00	01	11	10
0	1	0	0	1
1	1	0	1	1

$$D_{S1} = Q1.Q3 + \overline{Q2} \quad (4)$$

b. Karnaugh map and Boolean function of the second phase D flip-flop

Q3 \ Q1.Q2	00	01	11	10
0	0	1	1	1
1	0	0	0	0

$$D_{S2} = Q1.\overline{Q3} + Q2.\overline{Q3} \quad (5)$$

c. Karnaugh map and Boolean function of the third phase D flip-flop

Q3 \ Q1.Q2	00	01	11	10
0	1	1	0	0
1	1	1	1	0

$$D_{S3} = Q2.Q3 + \overline{Q1} \quad (6)$$

Table 1. The state table of the PWM control circuit

Current switching states (Q)			Next switching states (Q+1)			Output states		
Q1	Q2	Q3	Q1	Q2	Q3	D1	D2	D3
0	0	0	1	0	1	1	0	1
0	0	1	1	0	1	1	0	1
0	1	0	0	1	1	0	1	1
0	1	1	0	0	1	0	0	1
1	0	0	1	1	0	1	1	0
1	0	1	1	0	0	1	0	0
1	1	0	0	1	0	0	1	0
1	1	1	1	0	1	1	0	1

The circuit diagram of the proposed 120º phase shift circuit for a two-level three-phase inverter is presented in Figure 6.

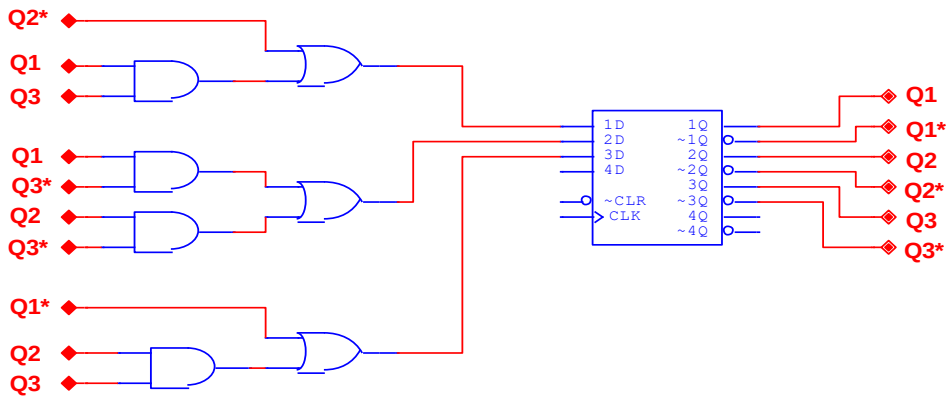


Figure 6. The proposed PWM control circuit for two-level three-phase inverters

3.3. Dead time control generation

To prevent a short circuit in the leg and the DC supply as well, the dead time must be included between the gate drive pulses for two IGBTs in one leg of the inverters [29]. A dead time circuit is a small interval Δt between the upper and lower switches in the same inverter leg used to reduce the switch losses and avoid the short circuit of the voltage source as shown in Figure 7. In addition, to avoid undesired harmonic spikes can be generated during the dead time case, which could cause electromagnetic interface issues [30], [31]. Figure 8 shows a dead-time control circuit for complementary power switches is used in this paper to generate a small dead time interval that is used to prevent the issue of the short circuit in the same phase leg.

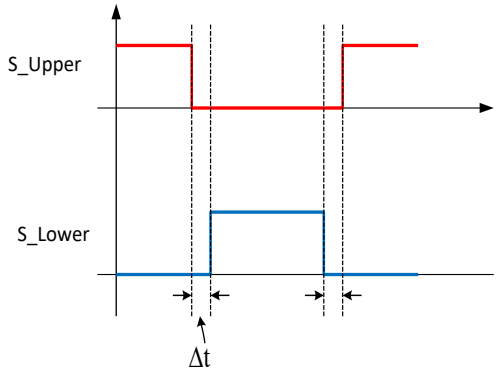


Figure 7. The dead time interval between complementary switches in the inverter phase leg

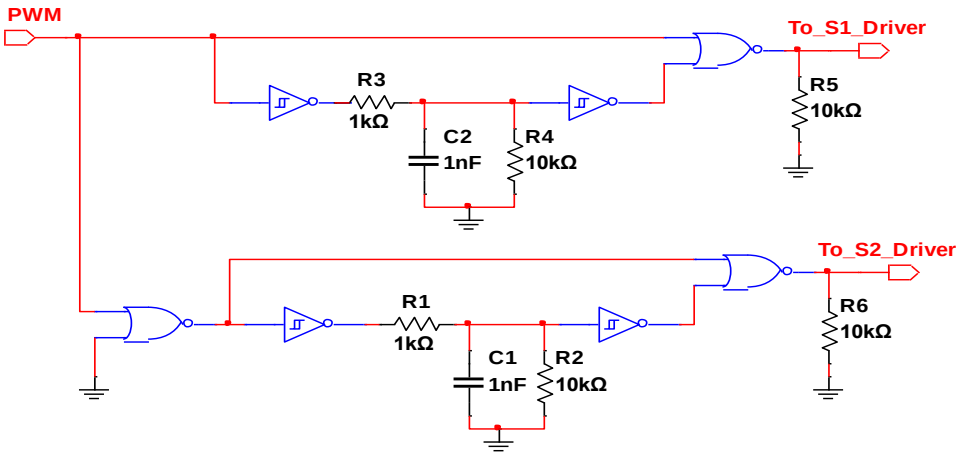


Figure 8. Dead time control circuit for complementary power switches

3.4. Gate driver circuit

A gate driver circuit is a power amplifier utilized to produce a high current from a low input current in order to operate the power transistors. Due to the low power output current of the proposed PWM control circuit, which fails to operate the power transistors of the inverter, this work uses the IR2112 as a gate driver circuit to amplify the current of the proposed control circuit to the needed voltage level to trigger the MOSFET. The IC IR2112 from the international rectifier is a high-speed, high-voltage power switch driver with independent high and low-side output channels [32], [33].

Figure 9 shows the final circuit diagram of the PWM control module for three-phase inverters including four stages; a square wave generator using a 555-timer, three-phase PWM generator with 120º phase shift, a dead-time control circuit which is used between two complementary switches in this paper, and the gate driver stage which is used by IC-IR2112.

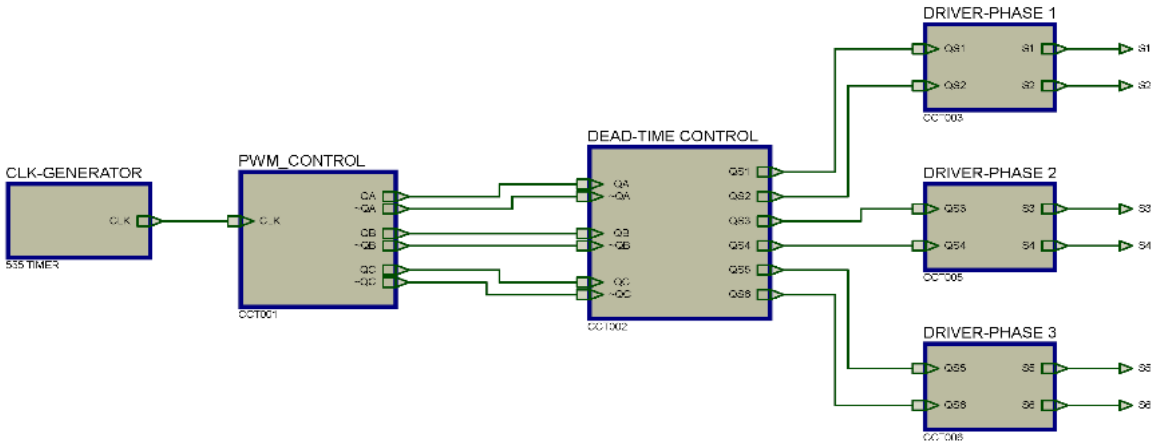


Figure 9. The proposed PWM control for three-phase inverters with 120º phase shift

4. SIMULATION RESULTS

To verify the performance of the proposed PWM control circuit in Figure 3, the design was simulated in PSIM and PROTEUS simulation tools. Three-phase inductive load in star connection load is used in the simulation, R=15 Ω, and L=10 mH. Figure 10 shows the simulation result of the dead-time control circuit. From Figure 10, the dead-time interval between both signals always remained. However, the control gate signals of the upper switches are presented in Figure 11.

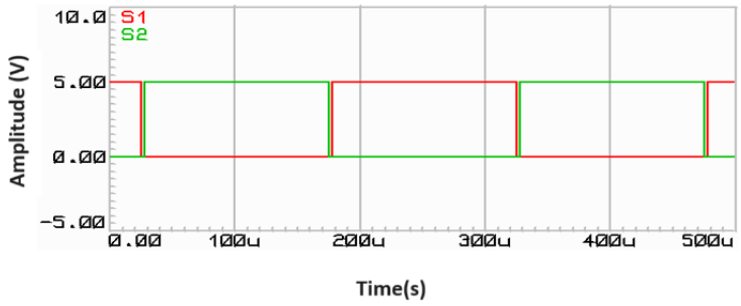


Figure 10. The simulation result of the dead-time for complementary switches

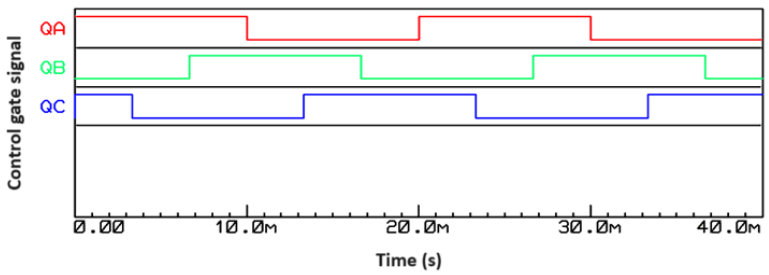


Figure 11. The output of the PWM control circuit signals for a three-phase inverter with 120º phase shift

As depicted in Figure 11, the output of the proposed PWM control circuit is 50 Hz with a 120º phase shift for three upper power switches. Figure 12 shows the simulation of the six control PWM signals. As indicated in Figure 12, the result of the proposed PWM module includes six PWM signals with a 120º for six power switches MOSFETs or IGBTs. Figure 13 shows the simulation result of line-to-line voltage and the fast fourier transform (FFT) analysis is presented in Figures 13(a) and (b) respectively. The total harmonic

distortion (THD) of the three-phase inverter line voltage in the simulation results without using filter is 31%. Figure 14 illustrates the phase current and its FFT spectrum analysis in Figures 14(a) and (b) respectively. The THD of the phase current without using a low-pass filter is 17%.

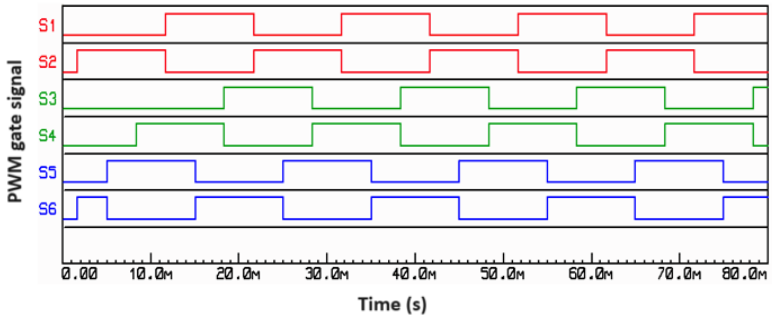
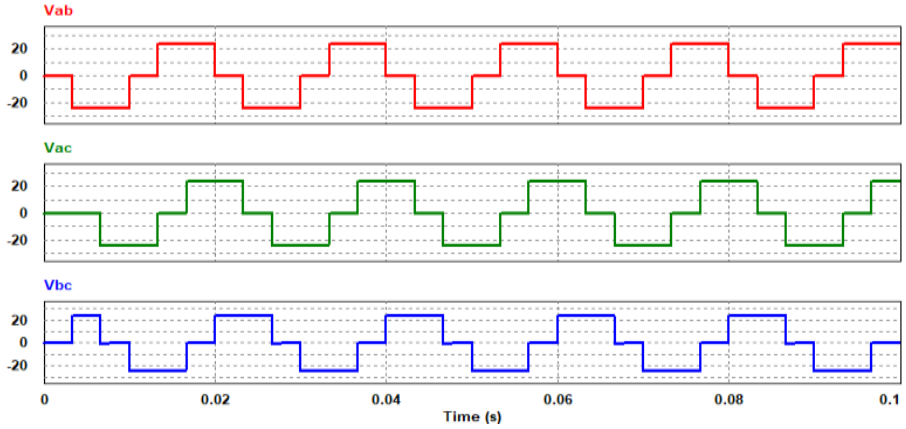
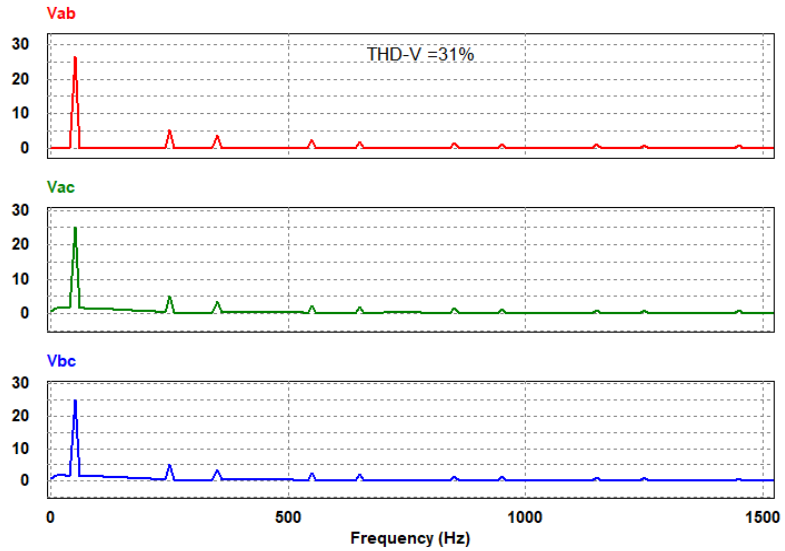


Figure 12. The simulation result of the proposed PWM module with six output signals for six power switches

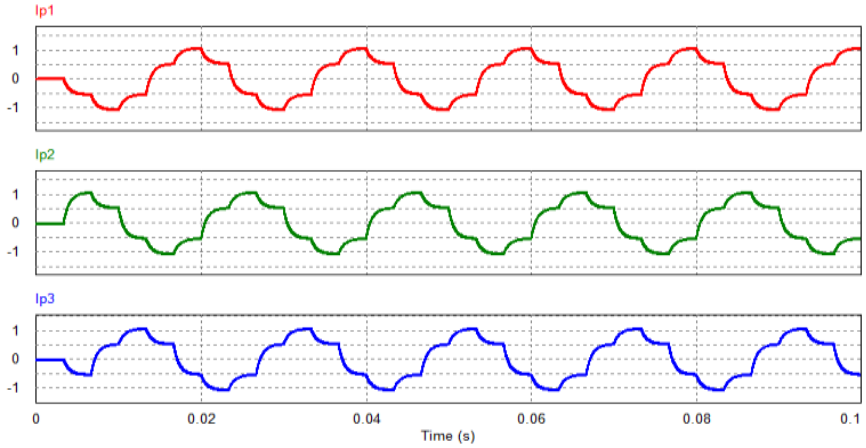


(a)

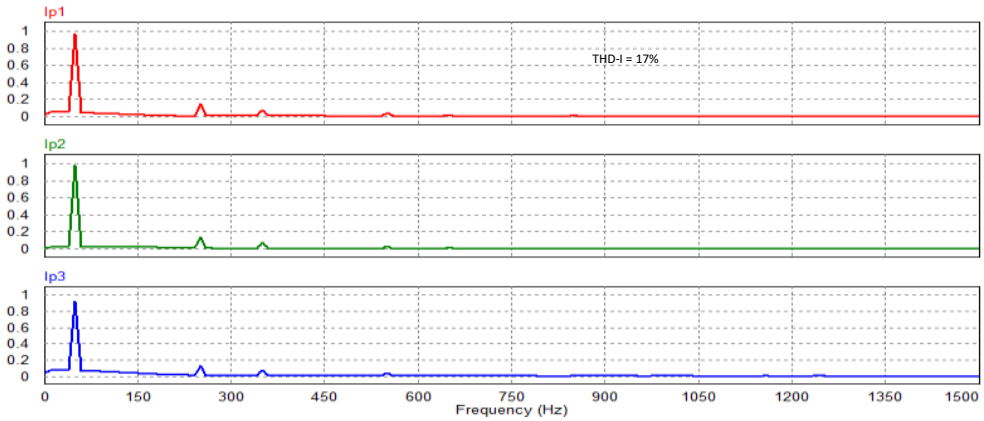


(b)

Figure 13. The simulation result of the three-phase inverter for; (a) line-to-line voltage and (b) FFT analysis



(a)



(b)

Figure 14. The simulation result of the three-phase inverter for; (a) phase current and (b) FFT spectrum analysis

5. EXPERIMENTAL RESULTS

To prove the performance of the proposed module, the laboratory experimental prototype for the PWM control board is implemented and tested with the two-level three-phase inverter as shown in Figure 15. Figure 16 shows the output of the proposed PWM control circuit is 50 Hz with a 120º phase shift for three upper power switches. In Figure 17, the output voltage waveform of the line-to-line voltage and the FFT analysis are presented. It is clear that from Figure 17, the result of the prototype module with the inverter is in close agreement with the simulation result compared with Figure 13.

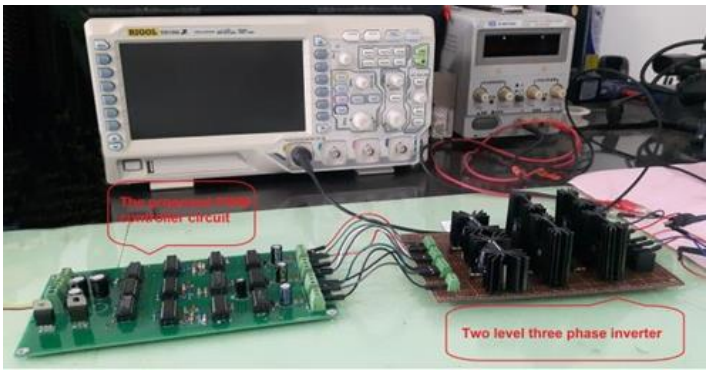


Figure 15. PCB prototype board of the PWM control circuit

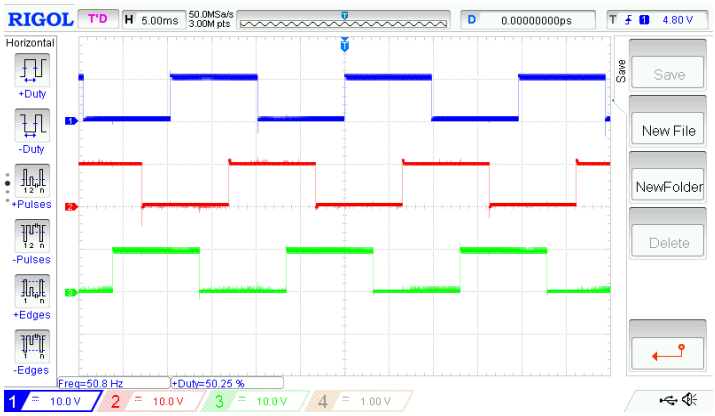


Figure 16. Experimental result of the proposed control module for the upper switches of the inverter

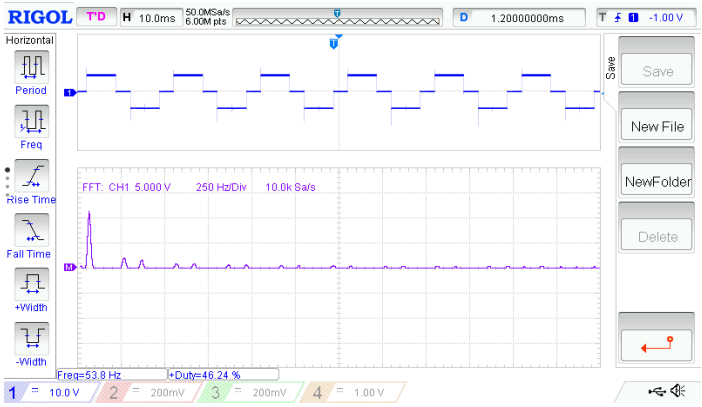


Figure 17. Experimental result of line-to-line output voltage using the proposed PWM control module and the FFT analysis

6. CONCLUSION

This paper proposed a single-input, multi-output 50 Hz PWM control circuit to control two-level, three-phase inverters. The proposed technique is easy to implement, low cost, and high performance. A 555-timer is used to generate a square wave as a single input to the proposed module, while the output is six PWM channels for the three-phase inverter to operate six power switches. D flip-flops and logic gates are the core components in the proposed technique which are used to generate the PWM pulses and 120° phase shift. A three-phase inverter has been used to evaluate the performance of the proposed control module in simulation and experimentally, and both results are in close agreement with almost identical values.

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