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Design of an efficient convolutional buck-boost converter for hybrid bioinspired parameter tuning

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ABSTRACT

Power-electronic systems with voltage boosts use buck-boost converters. These converters suppress current and invert voltage to improve voltage swing. Power-electronic systems with voltage boosts use buck-boost converters that suppress current and invert voltage to improve voltage swings. Researchers propose many converter models, but their total harmonic distortion (THD) limits their scalability. Harmonics from additional current components increase THD. The model filters excessive currents using inductor-based storage, capacitive filters, and resistive circuits. However, these models are unstable, reducing their performance in large converter circuits. This text proposes a novel convolutional neural network (CNN) with a hybrid bioinspired model based on genetic algorithm (GA) and particle swarm optimization (PSO) to overcome this limitation. Estimating internal buck and boost parameters efficiently reduces reverse currents. These parameters include inductor current ripple, recommended inductance, internal switch current limit, and switching frequency. The model finds low-power, high-efficiency buck-boost configurations based on these values. Incremental learning operations tuned the GA model, which was applied to many buck-boost configurations. The proposed model had a 5.9% lower delay, 16.2% lower harmonics, and 4.6% better power efficiency than state-of-the-art buck-boost models.

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1. INTRODUCTION

Design of low error and high-power efficiency buck-boost converters is a multidomain task, that involves the selection of transistor switching parameters, capacitor configurations, inductance values, and diode configurations. For a typical buck-boost converter with inverting buck-boost stage, the maximum duty cycle (D) is estimated via (1), wherein voltages at input, output and forward rectifier nodes are used.

$$D = \frac{-V_{out}+V_f}{-V_{out}+V_f+V_{in}} \quad (1)$$

Where V_{out}, V_{in} and V_f represents output voltage, input voltage, and forward voltage drop of the rectifier diode [1]. Thus, by varying the duty cycle, output voltage values can be modified, and boosted. This boost is due to a reduction in current values, which causes harmonic injection in the circuit. Fossil fuels, such as natural gas and coal, are currently the primary source of energy for nearly all human activity, particularly in the form of heat and power. In addition to being limited and non-renewable, these energy sources harm the environment, most

notably the climate, which is a major concern. As a result, it's critical to rethink how we use energy and look into alternative sources. Consequently, a buck-boost converter is used to sustain voltage levels. Windmills were modelled using permanent magnet synchronous generator (PMSG) and a buck-boost converter to control the electric pressure. Concept of a wind energy conversion unit with a boost converter and cascaded H-bridge multilevel inverter (CHB-MLI), which has a single DC input, this unit keeps the DC link voltage constant despite changes in wind pressure. The DC-DC output voltage is also maintained using a buck-boost converters. For grid-connected systems, managing the variable electric tension at the DC–DC link is critical. To reduce these harmonics, a wide variety of models are proposed by [2], and each of them have their own characteristics. These characteristics are reviewed in the section 2, wherein various nuances, advantages, limitations, and future research scopes of these models are discussed. Based on this discussion, it was observed that stability of these models is limited, due to which their performance is reduced when applied to large-scale converter circuits. To overcome this limitation, section 3 proposes design of the proposed buck-boost converter via bioinspired parameter tuning of circuit elements for reduced harmonics. Performance of this model is evaluated in section 4, and is compared with various state-of-the-art methods in terms of delay level, harmonic level, and power efficiency levels. Based on this evaluation, researchers can identify various characteristics of the proposed model, and identify its utility for their applications. Finally, this text concludes in section 5 with some interesting observations about the proposed model, and recommends various methods to further improve its performance.

2. LITERATURE REVIEW

A large number of buck-boost optimization models are proposed by researchers. For instance, work in [2]–[4] proposes particle swarm optimization (PSO) for PI based buck-boost converter, non-dominated sorting genetic algorithm for building a portable, highly efficient, and better performance converter, and a generalized optimized type-III controller by K factor method are discussed. These models assist in improving converter design by estimating multiple input and output configurations before the deployment of actual converter components. Extensions to these models are discussed in [5], [6] wherein novel modulation method for a four-switch buck-boost converter with reduced freewheeling current, and the use of lévy flight distribution and simulated annealing algorithms (LFDSA) for improving converter efficiency are proposed by researchers. These models also utilize stochastic processes for improving overall converter efficiency under different input and output conditions. An application of these configurations is discussed in [7], wherein electrolytic and capacitorless for parallel buck-boost converter is discussed, wherein researchers have incorporated parallel processing for improving the response time of buck and boost stages. This model is further extended in [8]–[10], wherein different bioinspired models, power factor correction (PFC) circuits, and hybrid buck-boost converter topologies are discussed. These models assist in augmenting buck-boost parameters in order to improve controller performance levels. Other methods that utilize model predictive control (MPC) [11], signal compensation and inner-outer convex combination for optimal control [12], and MPC with smooth mode transitions [13] are proposed by researchers. where researchers have showcased non auxiliary buck boost, adaptive tabu search, and artificial fish-swarm algorithm (AFSA) for optimization of converter performance. These models are further extended via use of maximum power point tracking (MPPT) [14], fuzzy proportional, integral derivative (PID) controller [15], complementary switching enabled cascaded boost-buck-boost (BS-BB) [16], and UPC strategy [17], which assists in low-power, and high-efficiency converter design with effective real-time control operations. But these models are highly stochastic, and cannot be applied to dynamic systems. To overcome these limitations, work in [18], [19] propose use of quadratic buck–boost converter, and high-gain buck-boost converter for better total harmonic distortion (THD) response, which makes it useful for real-time operations. Similar models are discussed in [20], [21], that aim at power converters, integrated high-quality rectifier regulator, and genetic algorithm (GA) with MLI and in [22]–[25] which aims at reducing harmonics from outputs, thereby improving conversion efficiency levels. Extensions to these models are discussed in [26]–[31] which propose use of switched reluctance motor (SRM), neutral point clamped (NPC), dynamic voltage restorer (DVR) topologies, high brightness light emitting diode (HB-LED), and non-isolated buck-boost dc/dc converters. Based on these methods, it can be observed that very few general-purpose optimization models are available for buck-boost converter performance improvement. Based on this observation, a novel buck and boost converter optimization model via bioinspired parameter tuning of circuit elements for reduced harmonics is proposed in the next section of this text. The model is evaluated on different input voltage ratings, and compared with various state-of-the art methods for estimating its performance under different circuit deployments.

3. PROPOSED METHOD

From the literature survey, it was observed that optimization of buck-boost converter requires efficient selection of internal components, or requires specialized circuitry for each type of optimization.

Component selection methods are capable of resolving context-sensitive issues, thus cannot be applied to general purpose buck-boost circuits. A very of these approaches consider modification of internal buck-boost component ratings based on input and output parameter swings. Based on these observations, this section proposes design of an efficient buck-boost converter via bioinspired parameter tuning of circuit elements for reduced harmonics. Overall flow of the proposed model is depicted in Figure 1, wherein connection of the GA model with buck-boost converter along with its feedback mechanism is depicted. This model is further tuned via use of a PSO model, which assists in improving mutation and crossover processes. The model initializes GA parameters, and sets up the circuit constraints. These include maximum input voltage swing, maximum output voltage swing, range of capacitor, range of inductor, and range of resistor. The values are processed via use of mutation and crossover processes, which assist in obtaining final buck-boost parameters. Selected parameters by the GA model are optimized via a convolutional neural network (CNN) classification process, which assists in improving temporal performance in terms of THD, delay and output power efficiency. These parameters are further optimized via an incremental learning process, and given to the underlying buck-boost circuitry for final deployment. The GA process can be described via the following steps:

a. Initialize GA parameters which include,
- Number of iterations (N_i),
- Number of solutions (N_s),
- Learning rate (L_r),
- Maximum rating of circuit components (Max_{val}),
- Minimum rating of circuit components (Min_{val}),
- Maximum range of input voltage swing ($Max(V_{in})$),
- Minimum range of input voltage swing ($Min(V_{in})$),

Initially mark all solutions as 'to be mutated'.

b. For each iteration in 1 to N_i
- Fix the input parameters for this iteration via (2):

$$\mathrm{V_{in}} = \mathrm{Stoch}\big(\mathrm{Min}(\mathrm{V_{in}}), \mathrm{Max}(\mathrm{V_{in}})\big) \quad (2)$$

Where Stoch represents a stochastic value, which is generated using a gold code pseudo random number generator (GPRNG).

- Based on this input value, for each solution in 1 to N_s

If the solution is marked as 'not to be mutated', then go to the next solution

Else, generate a new solution via the following process,

c. Generate component ratings via (3):

$$Rating_c = Stoch\big[Min_{valc}, Max_{valc}\big] \quad (3)$$

- This rating is evaluated for internal resistor, capacitor and inductor values, and deployed for the buck-boost circuit
- Based on these values, current and voltage levels of the circuit are evaluated, and its fitness function is estimated via (4):

$$f = \frac{\sqrt{\sum_{i=2}^{N}\left[\frac{I_{out_i}}{I_{out_1}}\right]^2} + \sqrt{\sum_{i=2}^{N}\left[\frac{V_{out_i}}{V_{out_1}}\right]^2}}{2} \quad (4)$$

Where N represents number of iterations, while I_{outi}, Vouti represents output harmonic current and voltage levels for the i^th harmonic. This process is repeated for all solutions, and a fitness threshold is evaluated via (5):

$$f_{th} = \frac{\sum_{i=1}^{N_s} f_i * L_r}{N_s} \quad (5)$$

- Solutions with fitness more than f_{th} are marked as 'to be mutated', while others are marked as 'not to be mutated'
- If more than 50% of solutions are marked as 'to be mutated', then repeat this iteration, else go to next iteration.

– At the end of this iteration, select the solution with minimum fitness, and tabulate its ratings as per Table 1 mentioned as example.
– Repeat this process for N_i iterations, and select solution with minimum fitness as the final parameter set for the given buck boost configuration.

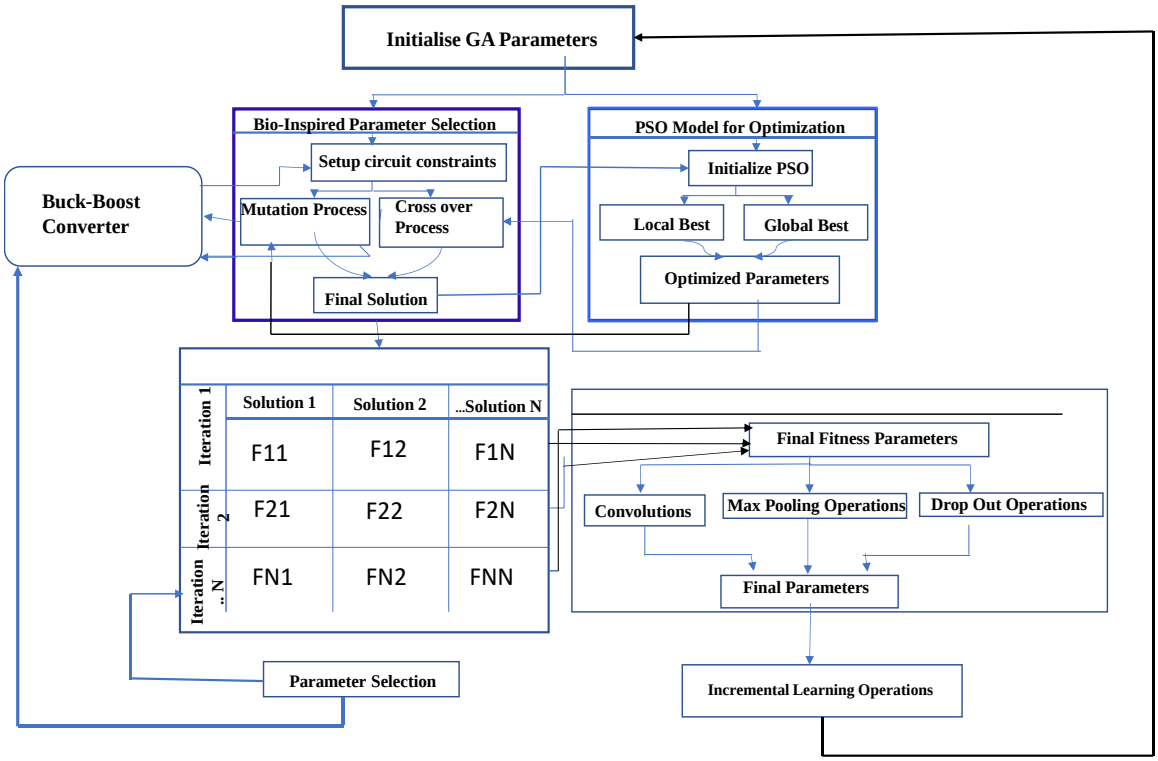

Figure 1. Overall flow of proposed GA model with CNN and incremental learning operations

Table 1. Iteration level parameter setting for optimized solutions

Input voltage (Volts)	Parameter ratings (ohms)	THD levels	Fitness value
40	10	5	4
45	20	6	4.5

These parameters are selected and deployed for the given buck-boost circuit, and its THD values are observed. If these THD levels are above a certain threshold, then the GA process is repeated again till required THD levels are obtained. The THD levels along with respective input voltage ranges can be used for any buck-boost converter for reduced harmonics. When this condition occurs, then a PSO model is activated, which assists in continuous tuning of GA learning rate. The PSO model works via the following process,

a. Initialize PSO parameters,
- Number of iterations (N_i)
- Number of particles (N_p)
- Cognitive learning rate (L_c)

b. Social learning rate (L_s) initialize PSO particles via the following process,
- Generate random values for learning rate via (6):

$$L_{r_i} = STOCH(0,1) \tag{6}$$

Where $STOCH$ represents a markovian stochastic process, and uses gold code random number generation for evaluating the learning rate values.
- For each value of L_r evaluate fitness value via the GA process, and mark this value as current particle velocity

- Mark best fitness of each iteration as $P(Best)$, and mark the minimum fitness as $G(Best)$

c. For each iteration in 1 to N_i perform the following,

- Evaluate new particle velocity via (7) as (7),

$$New(V) = C(V) * r + L_c[C(V) - PBest] + L_s[C(V) - GBest] \quad (7)$$

Where r and C(V) represents a random number, and current velocity of the particles.

- Based on this value of velocity, modify the value of L_r
- Select the particle with minimum fitness as $GBest$, and modify $PBest$ as per (8):

$$PBest = Old(V)\ if\ f_i > New(f_i), else$$

$$PBest = New(V) \quad (8)$$

d. Repeat this process for all iterations, and identify solution with minimum fitness, and use its learning rate for training the GA model.

e. Based on this process retrain the GA, and identify circuit component ratings. The selected ratings are given to a CNN model, that takes these ratings as input, and generates THD, power efficiency and delay as outputs. These outputs are compared with their respective thresholds, which assists in identification of retuning operations. The model is depicted in Figure 2 where, input features are extracted via a set of convolutional features via (9):

$$Conv_{out_i} = \sum_{a=-\frac{m}{2}}^{\frac{m}{2}} f(i-a) * ReLU\left(\frac{m}{2} + a\right) \quad (9)$$

Where f represents ratings selected by the GA layer, while $ReLU$ represents a rectilinear unit, which is used for activation of convolutional features.

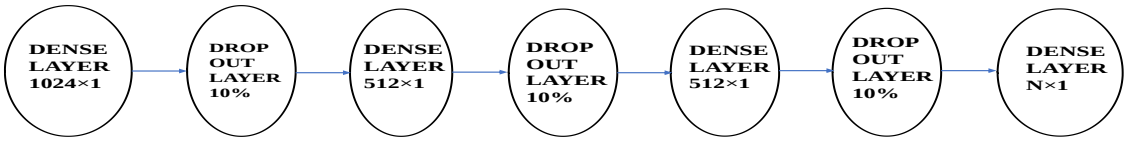

Figure 2. Design of the 1D CNN for retuning the GA model to achieve better performance

While extraction of features, the model uses parameters m, a, which represents window size and padding sizes, that are modified as per size of the convolutional layers. A dropout layer is used after these convolutional features, helping to exclude 10% of the features with lower variance values. As a result, it is noticed that the output features from these layers have reduced variance, which helps the final classification layer classify input signals into one of N classes. An activation function based on Soft Max is used for this, repeatedly using weights and bias levels via (10):

$$c_{out} = SoftMax\left(\sum_{i=1}^{N_f} f_i * w_i + b\right) \quad (10)$$

Where c_{out} indicates the output THD levels, while w_i and b represents convolutional weights and biases, that are tuned via a hyperparameter tuning process. Similar models are designed for estimation of delay and power efficiency classes, and are given to an incremental learning layer. This layer evaluates a correlation function between current classified output metrics, and target metrics via (11):

$$Corr_j = \frac{\sum_{i=1}^{N_{fTest}} F_{CNN_i} - F_{Target_i}}{\sqrt{\sum_{i=1}^{N_{fTest}} (F_{CNN_i} - F_{Target_i})^2}} \quad (11)$$

Where $N_{(fTest)} \in$(THD, power efficiency, delay), while F_{CNN} and F_{Target} represents output parameters by the CNN model and target output parameters respectively. If $Corr_j$>0.999, then there is no need to retrain the GA, otherwise the model is retrained, and new parameters are estimated for performance optimization purposes. The finalized ratings, are used by buck boost converters to improve their efficiency. Performance of this

model on different converters in terms of output delays, resulting harmonics, and power efficiency are discussed in the next section of this text.

4. RESULT ANALYSIS AND COMPARISON

The proposed bioinspired model is applicable for a wide variety of buck-boost converters, and can be deployed under multiple scenarios. The reason for this efficiency improvement is use of GA for estimation of optimum metrics that can be applied to the underlying buck-boost configuration for power efficiency optimizations. To evaluate performance of the proposed model, it was tested under different buck-boost input voltage configurations and circuit configurations. The circuits used for this evaluation can be observed from Figures 3(a) and 3(b) wherein general-purpose buck-boost controller is simulated, and its output efficiency metrics are evaluated. The evaluation is done on single buck-boost converter, and parallel buck boost converters, which assists in identification of model performance under different circuit types. These efficiency metrics include THD, efficiency of conversion (EC), and correction response time (CRT). These values were evaluated for PSO [2], and LFD SA [6] optimization models. The simulation was evaluated for different input voltages that range between 40 to 150 V, while output between 220 to 440 V was obtained, and values of THD, CE and CRT were estimated. The conversion efficiency was evaluated using as (12):

$$CE = \frac{\frac{In_{req}}{In_{act}} + \frac{Out_{req}}{Out_{act}}}{2} \quad (12)$$

Where In_{req} represents required input current and voltage, In_{act} represents actual input current and voltage, Out_{req} represents required output voltage and current, while Out_{act} represents actual output voltage and current.

There are situations in which the quantity of energy needed by the load is so low that it may be transmitted in a period of time that is less than the whole commutation period. In Figure 3(c), the amount of current flowing through the inductor drops to zero for a portion of the allotted time. The sole difference between this basic idea and the one explained before is that, at the conclusion of each commutation cycle, the inductor is totally de-. The output voltage equation is strongly impacted by the differential, despite the fact that it is rather little, which makes it useful for high-efficiency deployments. Based on this, performance of the model is evaluated in the next sub-sections of this text.

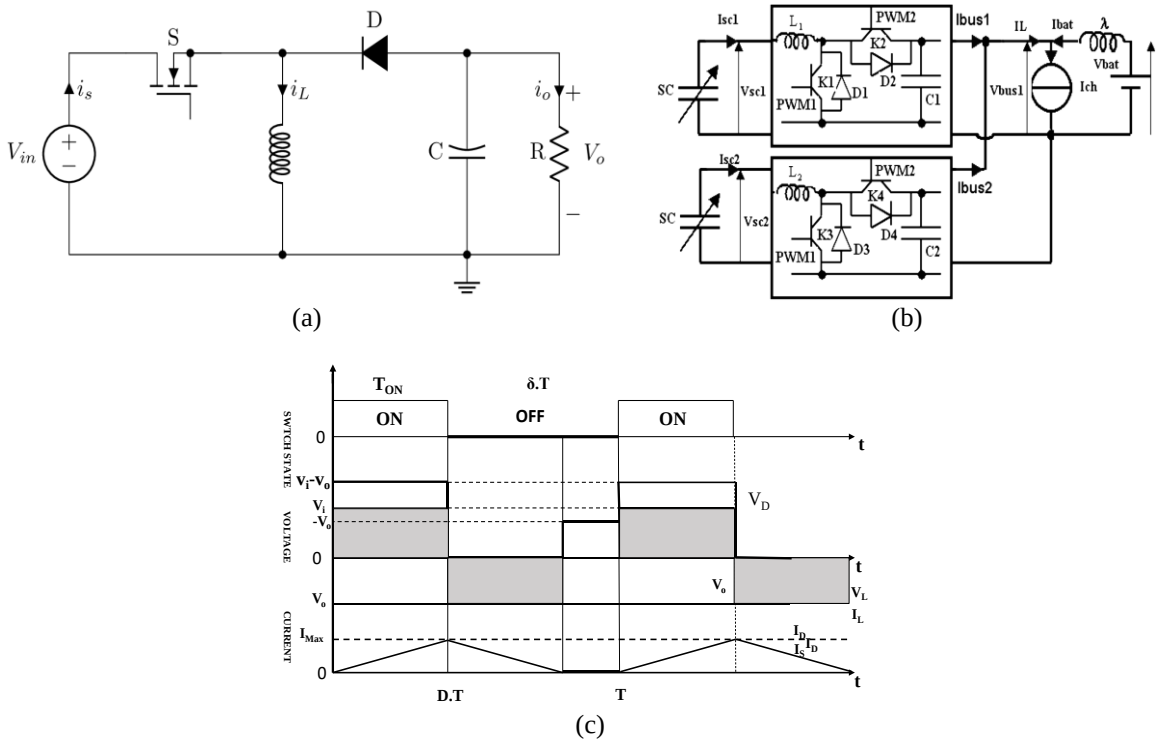

Figure 3. Buck-boost converter design and operation for evaluation (a) buck-boost converter used for evaluation, (b) parallel buck-boost converter used for evaluation, and (c) output of the circuit under different input variation levels

4.1. Efficiency estimation for single buck-boost converter

To estimate efficiency of single buck boost converter as depicted in Figure 3(a), both input and output current and voltage levels are used, which assists in estimating true performance of the underlying model. Based on these parameters, THD levels w.r.t. input voltage was evaluated, and can be observed from Table 2, it can be shown from this assessment and Figure 4 that the suggested model has a THD that is 34.6% lower when compared with PSO [2], and that it has a THD that is 20.5% lower when compared with LFD SA [6]. This enables it to be used in a broad range of different settings and applications. This is as a result of the use of bioinspired models, which aid in the gradual adjustment of the model for a variety of application scenarios. This is due to use of GA, and due to incorporation of voltage and current harmonic levels during estimation of internal component ratings. Similarly, results of average EC for different input voltages can be observed from Table 3.

From this evaluation and Figure 5, it is observed that the proposed model has 4.5% better EC when compared with PSO [2], and 5.3% better EC when compared with LFD SAB [6], thereby indicating its superior performance. This is because the ideal capacitor and indicator ratings were chosen, which contributes to the improvement of the overall efficiency of the process of increasing the input voltage levels. This finding also suggests that the suggested approach is applicable to a broad range of real-time deployments, all of which call for low THD values. In conclusion, the following are the observations that can be made from Table 4. As a result of this assessment, it was found that the suggested model had a quicker response efficiency performance than PSO [2] by 10.2% and LFD SA [6] by 25.3%. This indicated that the proposed model had a faster response efficiency performance. This is because the use of a bio-inspired model results in a reduced THD, which aids in the optimal selection of the component ratings for the internal circuitry under real-time scenarios.

Table 2. THD values of different input voltage ratings for single buck boost converter

Vin (V)	THD PSO [2]	THD LFD SA [6]	THD BS BB [16]	THD proposed
40	6.92	6.03	5.21	2.16
45	6.83	5.69	5.04	2.09
50	6.73	5.49	4.92	2.04
55	6.63	5.43	4.85	2.01
60	6.54	5.39	4.80	1.99
65	6.45	5.33	4.74	1.97
70	6.35	5.30	4.69	1.94
75	6.25	5.16	4.59	1.91
80	6.15	4.97	4.48	1.86
85	6.06	4.86	4.39	1.82
90	5.97	4.75	4.31	1.78
95	5.87	4.63	4.22	1.75
100	5.77	4.51	4.14	1.72
105	5.67	4.40	4.05	1.68
110	5.58	4.29	3.97	1.64
115	5.49	4.17	3.89	1.61
120	5.39	4.06	3.80	1.57
125	5.29	3.94	3.71	1.54
130	5.19	3.83	3.63	1.51
135	5.10	3.71	3.54	1.47
140	5.01	3.59	3.46	1.43
150	4.91	3.48	3.37	1.39

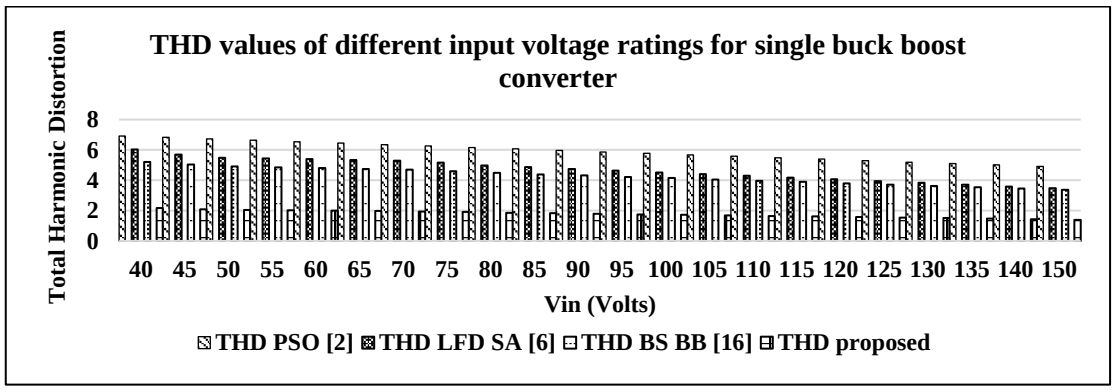

Figure 4. THD values of different input voltage ratings for single buck boost converter

Table 3. Average EC values for different input voltage ratings

Vin (V)	EC (%) PSO [2]	EC (%) LFD SA [6]	EC (%) BS BB [16]	EC (%) proposed
40	92.81	92.45	91.31	97.79
45	92.74	92.38	91.24	97.72
50	92.70	92.31	91.19	97.67
55	92.67	92.24	91.14	97.62
60	92.62	92.17	91.08	97.55
65	92.57	92.10	91.02	97.49
70	92.52	92.03	90.96	97.43
75	92.47	91.97	90.91	97.37
80	92.42	91.90	90.85	97.30
85	92.38	91.83	90.79	97.25
90	92.33	91.77	90.74	97.19
95	92.28	91.70	90.68	97.12
100	92.23	91.62	90.62	97.06
105	92.19	91.56	90.56	97.00
110	92.14	91.49	90.51	96.94
115	92.09	91.42	90.45	96.88
120	92.04	91.36	90.39	96.81
125	92.00	91.29	90.34	96.75
130	91.95	91.21	90.28	96.70
135	91.90	91.15	90.22	96.63
140	91.85	91.08	90.16	96.57
150	91.80	91.01	90.10	96.51

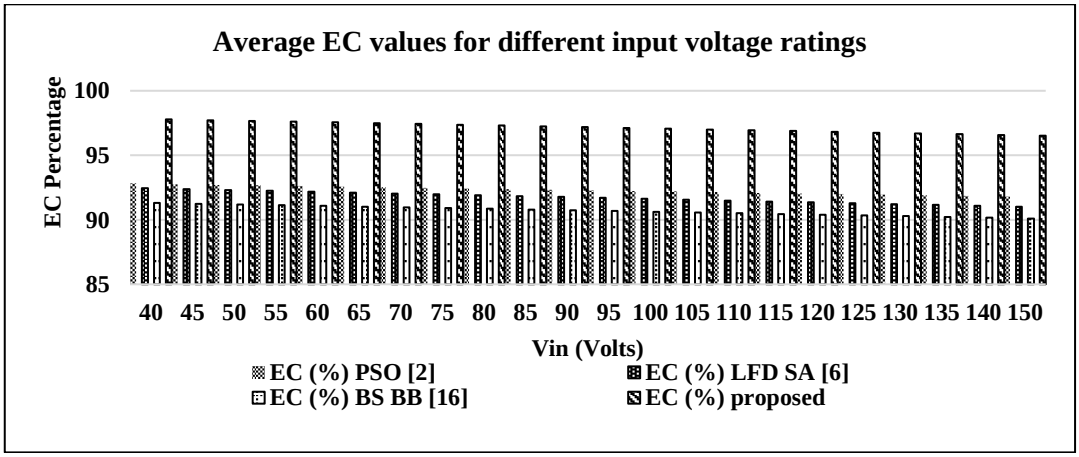

Figure 5. Average EC values for different input voltage ratings

Table 4. Average computational delay values for different input voltage ratings

Vin (V)	D (ms) PSO [2]	D (ms) LFD SA [6]	D (ms) BS BB [16]	D (ms) proposed
40	0.53	1.20	0.65	0.42
45	0.55	1.22	0.71	0.43
50	0.58	1.26	0.74	0.45
55	0.60	1.30	0.76	0.46
60	0.60	1.33	0.77	0.47
65	0.62	1.37	0.80	0.49
70	0.64	1.40	0.82	0.50
75	0.66	1.43	0.84	0.51
80	0.68	1.47	0.86	0.52
85	0.70	1.50	0.88	0.53
90	0.71	1.53	0.90	0.55
95	0.73	1.57	0.92	0.56
100	0.75	1.60	0.94	0.57
105	0.77	1.63	0.96	0.59
110	0.79	1.67	0.99	0.60
115	0.80	1.70	1.00	0.61
120	0.82	1.73	1.02	0.62
125	0.84	1.77	1.05	0.64
130	0.86	1.80	1.07	0.65
135	0.88	1.83	1.09	0.66
140	0.90	1.87	1.11	0.67
150	0.91	1.90	1.13	0.68

4.2. Efficiency estimation for parallel buck-boost converter

To estimate efficiency of parallel buck boost converter as depicted in Figure 3(b), both input and output current and voltage levels are used, which assists in estimating true performance of the underlying model. Based on these parameters, THD levels w.r.t. input voltage was evaluated, and can be observed from Table 5. From this evaluation and Figure 6, it is observed that the proposed model has 46.2% lower THD when compared with PSO [2], and 31.3% lower THD when compared with LFD SA [6], thus making it useful for a wide variety of applications. This is due to use of GA and PSO, and due to incorporation of voltage and current harmonic levels during estimation of internal component ratings. Similarly, results of average EC for different input voltages can be observed from Table 6.

From this evaluation and Figure 7, it is observed that the proposed model has 2.8% better EC when compared with PSO [2], and 6.5% better EC when compared with LFD SA [6], thereby indicating its superior performance. This is because the ideal capacitor and indicator ratings were chosen, which contributes to the improvement of the overall efficiency of the process of increasing the input voltage levels. This finding also suggests that the suggested approach is applicable to a broad range of real-time deployments, all of which call for low THD values. In conclusion, the following are the findings that can be obtained from Table 7 about the average computational latency for various input voltage levels.

Table 5. THD values of different input voltage ratings for parallel buck boost converter

Vin (V)	THD PSO [2]	THD LFD SA [6]	THD BS BB [16]	THD proposed
44	9.17	7.81	6.24	2.36
50	9.04	7.45	6.06	2.29
55	8.91	7.28	5.95	2.25
61	8.78	7.21	5.87	2.22
66	8.66	7.15	5.81	2.20
72	8.53	7.09	5.74	2.17
77	8.40	6.97	5.65	2.14
83	8.27	6.75	5.52	2.09
88	8.14	6.55	5.40	2.04
94	8.02	6.41	5.30	2.00
99	7.89	6.25	5.19	1.96
105	7.76	6.09	5.09	1.93
110	7.63	5.94	4.99	1.89
116	7.50	5.79	4.88	1.84
121	7.38	5.64	4.78	1.81
127	7.25	5.49	4.68	1.77
132	7.12	5.33	4.57	1.73
138	6.99	5.18	4.47	1.69
143	6.86	5.03	4.37	1.66
149	6.74	4.87	4.26	1.61
154	6.61	4.71	4.16	1.57
165	6.49	4.56	4.05	1.52

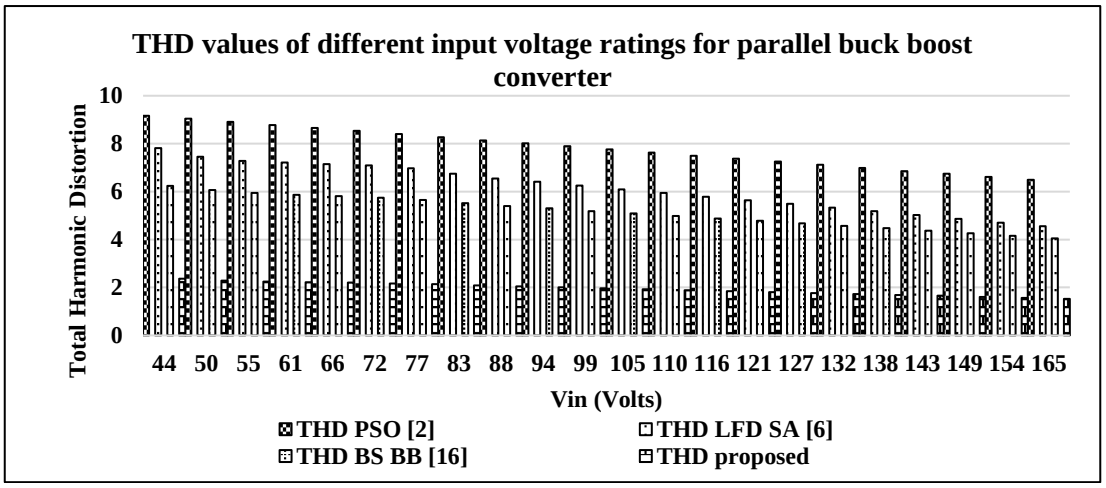

Figure 6. THD values of different input voltage ratings for parallel buck boost converter

Table 6. Average EC values of different input voltage ratings for parallel buck boost converter

Vin (V)	EC (%) PSO [2]	EC (%) LFD SA [6]	EC (%) BS BB [16]	EC (%) Proposed
44	95.15	94.78	92.96	98.25
50	95.10	94.71	92.90	98.19
55	95.06	94.64	92.85	98.14
61	95.02	94.57	92.80	98.08
66	94.97	94.50	92.74	98.01
72	94.92	94.43	92.68	97.95
77	94.87	94.36	92.62	97.89
83	94.82	94.29	92.56	97.82
88	94.77	94.22	92.50	97.76
94	94.72	94.15	92.45	97.71
99	94.67	94.09	92.39	97.64
105	94.62	94.01	92.33	97.58
110	94.57	93.94	92.27	97.52
116	94.53	93.87	92.21	97.46
121	94.48	93.80	92.15	97.40
127	94.43	93.73	92.09	97.33
132	94.38	93.67	92.04	97.27
138	94.33	93.59	91.98	97.21
143	94.28	93.52	91.92	97.15
149	94.23	93.45	91.86	97.09
154	94.18	93.38	91.80	97.03
165	94.13	93.31	91.75	96.97

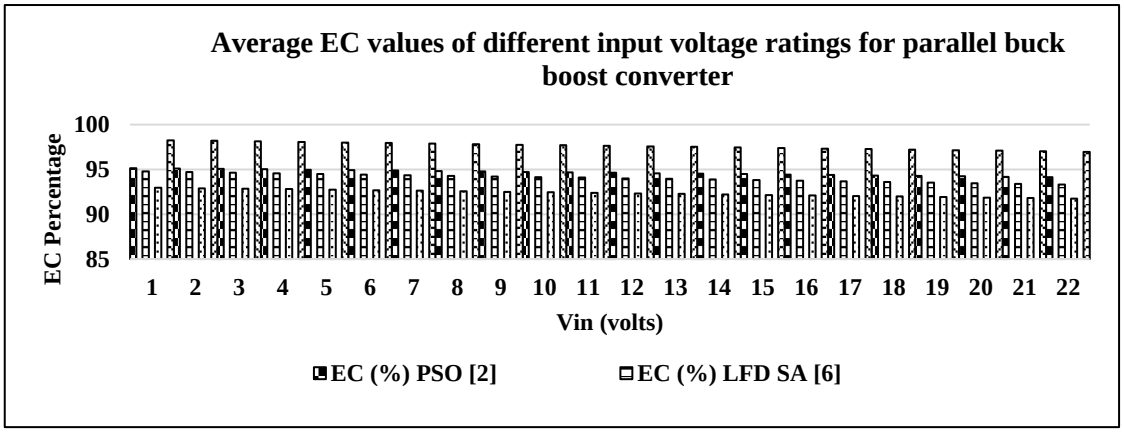

Figure 7. Average EC values of different input voltage ratings for parallel buck boost converter

Table 7. Average computational delay values of different input voltage ratings for parallel buck boost converter

Vin (V)	D (ms) PSO [2]	D (ms) LFD SA [6]	D (ms) BS BB [24]	D (ms) proposed
44	0.55	1.24	0.72	0.43
50	0.58	1.27	0.74	0.44
55	0.61	1.31	0.77	0.46
61	0.62	1.35	0.79	0.47
66	0.63	1.38	0.80	0.48
72	0.65	1.42	0.83	0.50
77	0.67	1.45	0.85	0.51
83	0.69	1.49	0.87	0.52
110	0.78	1.66	0.97	0.58
116	0.80	1.69	1.00	0.60
121	0.82	1.73	1.02	0.61
127	0.83	1.76	1.04	0.62
132	0.85	1.79	1.05	0.63
154	0.93	1.93	1.14	0.68
165	0.94	1.97	1.16	0.69

From this evaluation and Figure 8, it was observed that the proposed model was 23.1% faster than PSO [2], and 39.1% faster than LFD SA [6], thereby indicating its faster response efficiency performance. This is due to the low THD obtained via use of bioinspired model, that assists in optimum selection of internal component ratings. Due to this improvement, the proposed model is capable of being deployed for a wide variety of real-time applications. The model is currently evaluated on a single type of buck-boost

converter, but can be used for multiple buck-boost circuits without any reconfigurations. This indicates its high scalability performance under different circuit combinations.

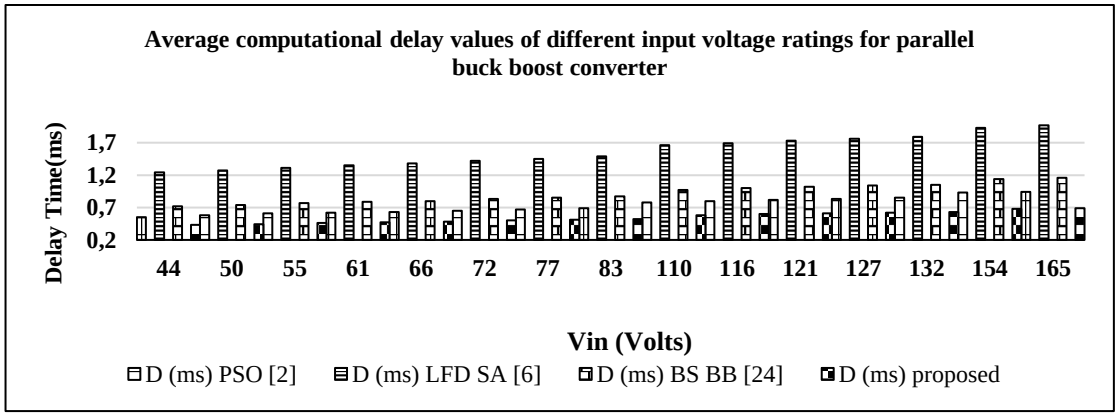

Figure 8. Average computational delay

5. CONCLUSION AND FUTURE WORK

The proposed bioinspired model uses maximum and minimum input ratings in order to estimate optimum values of internal buck boost circuit components. These values assist in reducing voltage and current THD, which improves overall circuit performance. Due to use of GA and PSO, a large number of stochastic values are generated for each input type, which are useful for analysing circuit performance under different input conditions. Based on this model, a standard buck-boost circuit was simulated, and it was observed that the proposed model had 34.6% lower THD when compared with PSO, and 20.5% lower THD when compared with LFD SA, thus making it useful for a wide variety of applications. Similar performance improvement was observed for EC, and response delay metrics. It was observed that the proposed model has 4.5% better EC when compared with PSO, and 5.3% better EC when compared with LFD SA, while, the proposed model was 10.2% faster than PSO, and 25.3% faster than LFD SA, thereby indicating its faster response efficiency performance. Due to these advantages, the proposed model is useful for a wide variety of buck-boost circuits. But the performance of the model was not valudated on other circuit, thus in future, researchers can validate performance of this bioinspired model on a variety of other buck boost circuits, which will assist in estimating its scalability for different applications. Moreover, researchers can also implement the model using deep learning techniques like CNNs, and Q-Learning for improving conversion performance, which was not done in this work, but it might increase overall response delays. Thus, researchers must identify redundancies in these models, which was not done, thus before deploying them for different buck-boost converter circuits.

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