❏ 4002

Efficient k-way partitioning of very-large-scale integration circuits with evolutionary computation algorithms

Rajeswari P.[1], Theodore Chandra S.[2], Smitha Sasi[1]

[1]Department of Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering, Bangalore, India
[2]Department of Electronics and Communication Engineering, Dayananda Sagar University, Bangalore, India

Article Info	ABSTRACT
	The standardization of very-large-scale integration (VLSI) physical architecture for VLSI chips and multichip platforms is now in its early stages of development. The purpose of VLSI partitioning is to divide the circuit into numerous smaller circuits with few connections in between. Partitioning is the fundamental problem in circuit design and division. The efficient method of evolutionary computation may be used to tackle the partitioning problem in VLSI circuit design. It provides a heuristic approach to solve this problem by exploring the solution space and incrementally improving the quality of the solutions. In order to obtain the shortest wire length (WL), area, and connections, an evolutionary optimized simulated annealing memetic algorithm (OSAMA) that incorporates one or more local search phases inside its evolutionary cycle was developed.

Corresponding Author:

Rajeswari P.
Department of Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering
Bangalore-78, Karnataka, India
Email: prajeswarisugans@gmail.com

1. INTRODUCTION

The integrated circuits known as very-large-scale integration (VLSI) circuits contain multiple transistors and other electronic components on an individual chip. Such circuits, which are frequently found in electronic gadgets that range from computers and cell phones to industrial equipment and automobiles, are created to carry out particular occupations or activities. In enabling the development of more advanced and potent electronic components, VLSI technology has played a crucial role in changing the electronics sector [1]. Modern technology has benefited greatly from the breakthroughs in computer, networking, and consumer electronics that VLSI circuits have made possible. Moore's Law has directed the constant advancement of VLSI technology, which has resulted in ever-increasing processing power and efficiency, enabling the development of complex electronic gadgets that are now an essential component of daily life [2]. The division of circuits into simpler and smaller components is an essential and crucial stage in VLSI architecture. To achieve optimal efficiency, save area and electrical consumption, and mitigate probable timing problems throughout chip design, circuit partitioning is essential. As technologies develop, VLSI circuit complexity rises, necessitating increasingly advanced partition strategies to satisfy the demanding requirements of contemporary electrical devices [3]. An innovative shift in the power sector regarding "integrated circuits (ICs)" with higher interconnections and complexities has been brought about by the growth of VLSI circuits. Since chip density increases, a range of challenging issues emerge that require being handled from the outset of the development phase, such as architecture clarity, evaluation, increased prevention, and optimal utilization of interconnects [4]. To manage these difficulties, improved design of

physical tools is necessary. One of the most significant steps in the actual construction of circuits based on VLSI is the division of the net list. To make planning, laying out, and testing easier, an electronic device is divided into smaller units called sub circuits [5].

Architecture design, logic design, practical layout, physical design, circuit design, packaging, and manufacture are the 8 interconnected stages of the VLSI design process. A summary requirement serves as the starting point of the process, and a complex layout that could have been tested, evaluated, and put into practice serves as the final product. This stage involves evaluating and adjusting the design's requirements about factors including performance, operability, manufacturing technology, and physical size [6]. This design level produces a register transfer level (RTL) description that is specified in a hardware description language (HDL). The employment of semiconductors, logic gates, wire, and other components is addressed at the development stage of the circuit design procedure. During the circuit design, the physical design level provides the circuit structure and converts it into an architectural specification. The next part goes into detail about this level. The design is then sent for manufacture, packaging, and testing of the IC as the following stage of design, to ensure that the system's requirements and standards have been fulfilled [7]. Reducing the number of exterior wires connecting each partition is an essential goal of the partitioned procedure. The following phase after partitioning is the design of floors and placement. The exact position of each of the sub-circuit elements within every partition is evaluated at this vantage point. The objectives of floor planning and installation are to arrange the elements in a manner that reduces the area by properly organizing their placement and to satisfy the practical requirements for the interconnectivity region. The result is sent to routing, where connections between the parts located inside partitions are made. The process of routing can be characterized as one that chooses the most efficient paths within a given routing region to connect the elements across or between partitions [8].

2. METHOD

Explaining graph partitioning issues are a typical notation for cases of circuit partitioning. Conventional mathematical representations of circuits are graphs, where nodes stand for individual circuit elements and edges reflect the relationships between components in Figure 1 [9], [10]. The following is a statement of the partitioning problem based on the graph concept: find $S(C,A)$ $S = (C,A)$ for the vertices to $c \in C$ through dimensions $g(c)g(c)$ related by border boundaries $a \in A$ with masses $u(a)$ are divided into r subsets $c1, c2, \ldots\ldots cr$ with $\bigcup_{j=1}^{r} cj = c$ $cj \cap c = 0$ for $j \neq i$. It is possible to cut particular relations to divide the circuit depicted in Figure 2 into k subsets [11].
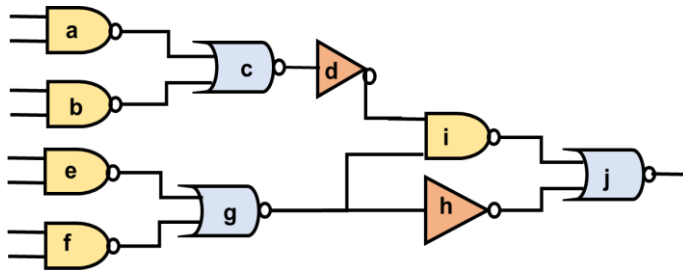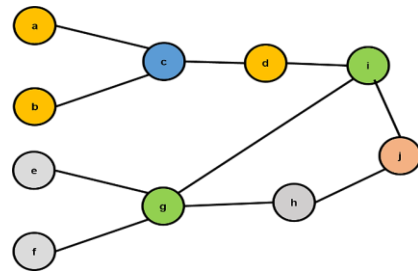

Figure 1. A logic circuits

Figure 2. A graphical representation of the logic circuit

The cost of the two partitions is the relevant metric, and it may be written as (1):

$$cost = \sum_{j=1}^{r} \quad \sum_{i=1}^{r} \quad V_{ji}, \text{where} j \neq i \tag{1}$$

Dividing a collection into exactly two separate parts is the simplest possible partition problem. In contrast, the complexity of this example is already excessive despite identical nodes and unit border masses. Indeed, given a system with 2 m nodes, the number of neutral bipartitions is (2) [12]:

$$\sum_{j=0}^{r} \quad n_j = \sum_{i=0}^{r} \quad m_i \tag{2}$$

Where, j and i the vertices of edges need to be labeled and n_j and m_i are listings of nodes in each partition [13]. Gain $\Delta s(C,U)$ in the process of exchanging two nodes C and U is the overall savings from this kind of trading rise. A positive outcome ($\Delta s > 0$) suggests a lessening of cost-cutting measures, contrasted with a positive loss ($\Delta s < 0$) suggests a rise in value. The benefit of exchanging nodes C and W is (3):

$$\Delta s(C,U) = J_c + J_u - 2a(C,U) \tag{3}$$

J_c and J_u increase at nodes C and U, and their equivalent nodes, and $a(C, U)$ represents the importance of the relationship among nodes C and U. In the event where C and U share an edge $a(C, U) = 1$; else, $a(C, U) = 0$ [14], [15].

The maximum gain a pair contributes in a particular phase with all possible node swapping is indicated by Δs_{max}. If each partition contains r nodes, then, the sum of all possible hops between nodes is r^2. Thus,

$$\Delta s_{max} = (\Delta s_j), \text{where} j = 1, 2, \dots r^2 \tag{4}$$

Again, listing each partition and selecting the best one is impracticable for moderate quantities of n in (4), and it approaches difficult in greater circuits. Algorithms using heuristics are a useful tool for dealing with such issues. These algorithms typically produce an approach that is not optimal but is quick and easy to implement [16]. All of these algorithms produce the same solutions to any specific problem. Stochastic algorithms, which depend on chance, produce different results for the same issue with each iteration. Various common partition issues can be solved using known stochastic techniques [17].

2.1. Optimized simulated annealing memetic algorithm

Both simulated annealing (SA) and memetic algorithms (MA) are optimization methods for locating approximations of solutions to challenging issues [18], [19]. To improve the search capabilities and effectiveness of the optimization process, an optimized simulated annealing memetic algorithm (OSAMA) can be created by combining these two methods. SA mimics cooling material to a low-energy state and is modeled after the metallurgical annealing procedure [9], [20], [21]. It probabilistically searches the solution space and gradually progresses towards better solutions, allowing for sporadic uphill climbs to avoid local maxima. OSAMA is particularly well-suited for addressing issues with harsh and multimodal terrain thanks to this hybrid approach's ability to balance exploration and exploitation efficiently [22], [23].

3. RESULTS AND DISCUSSION

In this the suggested method OSAMA methodological approach in comparison to existing models, like "parallel particle swarm optimization with sequence pair (P-PSO-OPFP) [24], [25], nature-inspired hybrid optimization algorithm (BIOA-OPFP) [26], fixed-outline floor planning (LOA-OPFP) [27], and hybrid bio-inspired whale optimization and adaptive bird swarm optimization optimal partitioning and FloorPlanning (Hyb-BI-WO-ABSO-OPFP) [7]" techniques, all calculated with the benchmark. The S1196 and S1238 and the S3350 and the S8378 benchmark circuits (BC) are used in this study. The design parameters are then used to generate evaluation metrics such as "area, wire length (WL), delay, speed, and power value". Table 1 displays the simulation parameters. Minimizing routing WL and minimizing dead area on the floor layout is a couple of ways in which costs can be reduced when designing VLSI circuits.

Table 1. Simulation parameters

Parameter	Value
Maximum value	+1
Benchmark circuit (BC)	s4
Minimum value	-1
Number of iterations	500
Random number	(0 or 1)

3.1. Area

To interconnect elements across or inside segments yet consuming a minimum quantity of space, router can be defined as a process that selects the optimal routes across the path selection domain. VLSI area value comparison is the process of determining the corresponding dimensions of chips based on their respective circuit designs, architectures, or implementation techniques. When optimizing a VLSI design, comparing area values is an essential initial phase that allows engineers to make educated judgments that lead to high-quality, low-cost chips. Figure 3 and Table 2 display a comparison of area values for the benchmark. Area reduction of 35.26%, 22.31%, 29.05%, and 32.10% were achieved for the S1196 benchmark design using the suggested OSAMA technique, reduced surface area by 30.25%, 32.05%, 40.28%, and 28.28% for the S1238 BC, the S3350 BC is 22.35%, 24.57%, 23.58%, and 29.65% less in size, reduced surface area by 21.45%, 23.56%, 24.76%, and 29.27% for the S8378 BC, than existing techniques as (P-PSO-OPFP, BIOA-OPFP, LOA-OPFP, and Hyb-BI-WO-ABSO-OPFP). In this study, our proposed method has less area compared to an existing method.
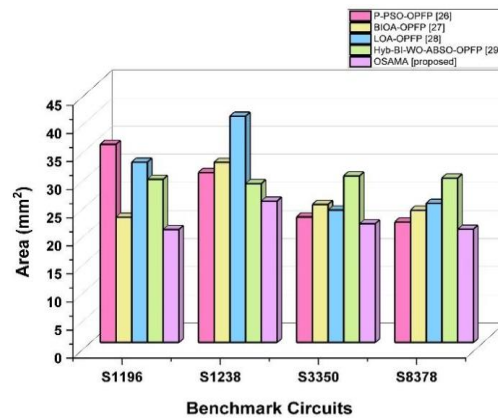
Figure 3. Benchmark value comparison in an area

Table 2. Comparison of area

Methods	S1196 (%)	S1238 (%)	S3350 (%)	S8378 (%)
P-PSO-OPFP	35.26	30.25	22.35	21.45
BIOA-OPFP	22.31	32.05	24.57	23.56
LOA-OPFP	32.10	40.28	23.58	24.76
Hyb-BI-WO-ABSO-OPFP	29.05	28.28	29.65	29.27
OSAMA [proposed]	20.11	25.16	21.12	20.15

3.2. Delay

VLSI circuit design optimization additionally depends significantly on comparing delay values. The delay of a VLSI circuit is the amount of time required for a signal to travel from its input to it is output. The essential element to high-performance and rapid operation of integrated circuits is minimizing signal propagation delay. The delay value comparison is shown in Figure 4 and Table 3. In comparison to established techniques like "P-PSO-OPFP, BIOA-OPFP, Hyb-BI-WO-ABSO-OPFP, and LOA-OPFP", the suggested technique OSAMA reduces delays by 40.28%, 23.58%, 27.38%, and 25.49% for the S1196 BC, 36.24%, 30.27%, 37.59%, and 22.05% for the S1238 BC, 21.04%, 19.68%, 18.65%, and 17.45% for the S3350 BC, 32.05%, 31.07%, 29.63%, and 27.56% for the S8378 BC. In the VLSI circuit, it provides a low-level delay comparison between a suggested technique and an existing method.
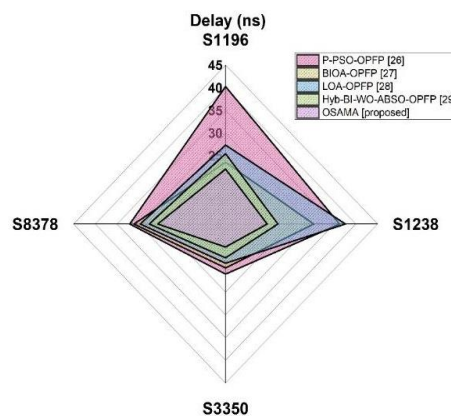

Figure 4. Comparison of benchmark delay

Table 3. Comparison of delay

Methods	S1196 (%)	S1238 (%)	S3350 (%)	S8378 (%)
P-PSO-OPFP	40.28	36.24	21.04	32.05
BIOA-OPFP	23.58	30.27	19.68	31.07
LOA-OPFP	27.38	37.59	18.65	29.63
Hyb-BI-WO-ABSO-OPFP	25.49	22.05	17.45	27.56
OSAMA [proposed]	22.10	19.58	15.07	25.60

4. CONCLUSION

VLSI chips contain numerous transistors and other electrical components. The challenge of dividing VLSI circuits is critical and difficult to the design and execution of integrated circuits. Partitioning is the technique of dividing a big circuit into more manageable sections to better optimize its performance metrics and design goals. In this research, we show that the OSAMA may be used to generate optimal results for layout and partitioning for VLSI. The S1196, S1238, S3350, and S8378 BCs were used in the benchmark evaluation. The proposed OSAMA algorithm can 20.11%, 25.16%, 21.12%, and 20.15% area is lower, 22.10%, 19.58%, 15.07%, and 25.60% lower delay.

REFERENCES

[1] M. Bansal, R. Arora, and R. Bharti, "VLSI layout: concept to realization," in *Proceedings-International Conference on Applied Artificial Intelligence and Computing, ICAAIC 2022*, 2022, pp. 1590–1596, doi: 10.1109/ICAAIC53929.2022.9792835.

[2] F. H. Khan, M. A. Pasha, and S. Masud, "Advancements in microprocessor architecture for ubiquitous AI-an overview on history, evolution, and upcoming challenges in ai implementation," *Micromachines*, vol. 12, no. 6, 2021, doi: 10.3390/mi12060665.

[3] S. M. Abbas, T. Tonnellier, F. Ercan, and W. J. Gross, "High-throughput VLSI architecture for GRAND," *IEEE Workshop on Signal Processing Systems, SiPS: Design and Implementation*, 2020, doi: 10.1109/SiPS50750.2020.9195254.

[4] S. Shreyanth, D. S. Harshitha, and S. Niveditha, "Implementation of machine learning in VLSI integrated circuit design," *SN Computer Science*, vol. 4, no. 2, 2023, doi: 10.1007/s42979-022-01580-5.

[5] V. S. Chakravarthi and S. R. Koteshwar, "Introduction to design of system on chips and future trends in VLSI," *SoC Physical Design*, pp. 1–20, 2022, doi: 10.1007/978-3-030-98112-9_1.

[6] J. K. Kurian, "Study on recent approaches of power optimization techniques in VLSI design," in *IET Conference Proceedings*, 2023, pp. 54–58, doi: 10.1049/icp.2023.1417.

[7] R. Karthick, A. Senthilselvi, P. Meenalochini, and S. S. Pandi, "An optimal partitioning and floor planning for vlsi circuit design based on a hybrid bio-inspired whale optimization and adaptive bird swarm optimization (WO-ABSO) algorithm," *Journal of Circuits, Systems and Computers*, vol. 32, no. 8, 2023, doi: 10.1142/S0218126623502730.

[8] I. Oliveira, M. Danigno, P. F. Butzen, and R. Reis, "Benchmarking open access VLSI partitioning tools," *2021 IEEE 12th Latin American Symposium on Circuits and Systems, LASCAS 2021*, 2021, doi: 10.1109/LASCAS51355.2021.9459131.

[9] P. Rajeswari, T. S. Chandra, and A. K. Kumar, "Synthesis of VLSI structural cell partitioning using genetic algorithm," *Advances in Intelligent Systems and Computing*, vol. 1270, pp. 279–287, 2021, doi: 10.1007/978-981-15-8289-9_26.

[10] N. Thakur, S. Saxena, and D. Kumar, "Circuit simulation techniques of VLSI circuits," in *International Conference on Electronic Design Innovation and Technology-2015*, 2015.

[11] G. Luo, X. Chen, and S. Nong, "Net clusting based low complexity coarsening algorithm in k-way hypergraph partitioning," *Journal of Physics: Conference Series*, vol. 2245, no. 1, 2022, doi: 10.1088/1742-6596/2245/1/012019.

[12] L. Lin, T. Wu, and Z. Zhang, "A diameter-based model of the rectilinear partitioning problem in VLSI physical design," *Proceedings-2020 Chinese Automation Congress, CAC 2020*, pp. 2610–2615, 2020, doi: 10.1109/CAC51589.2020.9327644.

[13] J. Rodriguez *et al.*, "Circuit partitioning with path delay-based minimization," in *EURO 2021-31st European conference on operational research*, 2022.

[14] M. A. Sebak, M. A. Fawzy, M. A. Ibrahim, and R. G. Elsaid, "A greedy-simulated annealing approach for placement of VLSI circuits".

[15] B. Srinivasan, R. Venkatesan, B. Aljafari, K. Kotecha, V. Indragandhi, and S. Vairavasundaram, "A novel multicriteria optimization technique for VLSI floorplanning based on hybridized firefly and ant colony systems," *IEEE Access*, vol. 11, pp. 14677–14692, 2023, doi: 10.1109/ACCESS.2023.3244346.

[16] K. Lakshmanna, F. Shaik, V. K. Gunjan, N. Singh, G. Kumar, and R. M. Shafi, "Perimeter degree technique for the reduction of routing congestion during placement in physical design of VLSI circuits," *Complexity*, 2022, doi: 10.1155/2022/8658770.

[17] A. Agnesina, S. Pentapati, and S. K. Lim, "A general framework for VLSI tool parameter optimization with deep reinforcement learning," *Workshop on Machine Learning for Systems*, pp. 1–6, 2020.

[18] S. Lamichhane, S. Peng, W. Jin, and S. X. D. Tan, "Fast electrostatic analysis for VLSI aging based on generative learning," *2021 ACM/IEEE 3rd Workshop on Machine Learning for CAD, MLCAD 2021*, 2021, doi: 10.1109/MLCAD52597.2021.9531320.

[19] S. N. Hussain and K. H. Kishore, "Heuristic approach to evaluate the performance of optimization algorithms in vlsi floor planning for asic design," *Studies in Computational Intelligence*, vol. 885, pp. 213–225, 2020, doi: 10.1007/978-3-030-38445-6_16.

[20] S. D. Nadella, A. Israel, G. Reddy, N. Rao, and M. Rao, "A dual threshold voltage modified dynamic power cutoff technique to consolidate leakage and speed in a VLSI subsystem," in *2019 IEEE International Conference on Electronics, Computing and Communication Technologies, CONECCT 2019*, 2019, doi: 10.1109/CONECCT47791.2019.9012898.

[21] Y. H. Lee, C. H. Kuei, Y. Z. Kao, and S. S. Fan Jiang, "Algorithm and VLSI architecture designs of a lossless embedded compression encoder for HD video coding systems," *Journal of Circuits, Systems and Computers*, vol. 30, no. 4, 2021, doi: 10.1142/S021812662130004X.

[22] A. R. Chadachana and D. S. Chandra, "An investigation on basic concepts of particle swarm optimization algorithm for VLSI Design," *International Journal of Engineering and Techniques*, vol. 4, no. 1, 2018.

[23] P. Rajeswari and S. T. Chandra, "A survey on an optimal solution for VLSI circuit partitioning in physical design using DPSO and DFFA algorithms," in *Proceedings of the International Conference on Intelligent Sustainable Systems, ICISS 2017*, 2018, pp. 868–872, doi: 10.1109/ISS1.2017.8389301.

[24] P. Rajeswari and T. S. Chandra, "Partitioning of VLSI circuits on the basis of standard genetic algorithm and comparative analysis of partitioning algorithms," *SSRG International Journal of Electrical and Electronics Engineering*, vol. 9, no. 12, pp. 126–133, 2022, doi: 10.14445/23488379/IJEEE-V9I12P111.

[25] S. J. Basha, and B.A.Raheem, In *ICDSMLA 2019: Proceedings of the 1st International Conference on Data Science, Machine Learning and Applications*, Springer Singapore, 2020, pp. 1959-1967, doi: 10.1007/978-981-15-1420-3_200.

[26] H. Abderazek, F. Hamza, A. R. Yildiz, and S. M. Sait, "Comparative investigation of the moth-flame algorithm and whale optimization algorithm for optimal spur gear design," *Materials Testing*, vol. 63, no. 3, pp.266-271, 2021, doi: 10.1515/mt-2020-0039.

[27] B. S. Yıldız, N. Pholdee, S. Bureerat, M. U. Erdaş, A. R. Yıldız, and S. M. Sait, "Comparision of the political optimization algorithm, the Archimedes optimization algorithm and the Levy flight algorithm for design optimization in industry," *Materials Testing*, vol. 63, no. 4, pp. 356-359, 2021, doi: 10.1515/mt-2020-0053.

BIOGRAPHIES OF AUTHORS

Rajeswari P. 🆔 ⑧ sc ⟳ received the Bachelor of Engineering degree from Government College of Technology, Coimbatore and Master's degree in VLSI Design from Anna University, Chennai. She is currently pursuing the Ph.D. degree with Department of Electronics and Communication Engineering, Dayananda Sagar University, Bangalore-78. Currently working as an assistant professor in Department of ETE, DSCE, Bangalore-78. Her research interests include embedded system design, VLSI signal processing, circuit optimization, and CAD algorithms for VLSI architectures. She can be contacted at email: prajeswarisugans@gmail.com.

Theodore Chandra S. 🆔 ⑧ sc ⟳ received his Ph.D. from Anna University, Chennai. He has completed his Bachelor of Engineering in Electronics and Communication Engineering and Masters of Engineering with specialization in Communication Systems from Anna University, Chennai. His research interest includes semiconductor device modeling and simulation, high electron mobility transistors, and nanowire transistors. He is a recipient of senior research fellowship from the Council of Scientific and Industrial Research (CSIR), Government of India, New Delhi. He is elevated to the grade of IEEE senior member in April 2019. He is a member of technical societies like IEEE, ECS, IEICE and IAENG. He has completed a CEP course on "semiconductor technology and manufacturing" conducted by IIT Bombay. He is a certified trainer for the Centre of Competence for Automation Technologies-Joint Initiative of Bosch Rexroth and Dayananda Sagar University. He can be contacted at email: Theodore-ece@dsu.edu.in.

Smitha Sasi 🆔 ⑧ sc ⟳ working as an associate professor in the Department of Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering has about 17 years of teaching experience. She received her B.Tech. degree in Information Technology from Calicut University and M.Tech. degree in digital communication and networking with rank from Visvesvaraya Technological University, Belagavi, Karnataka. She is received Doctoral Degree in Cryptography from Visvesvaraya Technological University. She has published research papers in refereed international journals and research papers in the proceedings of various international conferences. She received funds from various funding agencies in the cryptography and security domain. She is authored various book chapters in the area of cryptography. She can be contacted at email: smitha-tce@dayanandasagar.edu.