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Comparative analysis of meta heuristics algorithm for differential amplifier design

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ABSTRACT

The design of analog circuits is very essential for the development of system design based on electronics as the world is analog in nature. Furthermore, performance of emerging products depends on analog circuits for reduction of power dissipation and improvement of speed. Though in the system on chip (SoC) analog circuit consumes less, it is more complex to design it due to the analog circuit nature complexity. The job of the evolutionary algorithm (EA) in the process of optimization of an analog circuit based on complementary metal oxide semiconductor (CMOS) is to get the appropriate values that can be used for the design parameters of the given circuit in such a way such that all the targeted specification of the given circuit can be obtained. The chaotic serial particle swarm optimization (CSPSO) and cuckoo search (CS) algorithms are lower than to those found through the particle swarm optimization (PSO) and differential evolution (DE) algorithms. The CS algorithm obtained all the desired specifications with less power dissipation and the least total transistor area compared to those attained by the DE and PSO algorithms.

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1. INTRODUCTION

Analog circuit is main backbone of any electronic gadget that may be utized in our daily life, such as consumer product, telecommunications, and business. So that design of any analog circuit is very crucial task. Number of attempts is made by different technologist and researchers to optimize the design of analog circuit. For the proper design of analog circuit, there are three stages suggested to obtained desired specifications and physical layout of the analog circuit at the achematic level [1], [2]. Modern system on chips (SoCs) contains about 75% of analog components to interact with real world [3]. At the same time only about 10% of total chip area covered by this analog circuit. So, rest of about 90% of total time required for the chip design and validation due to the advancement in IC technology [4]. Many researchers and research institutions across the globe are trying for development and improvement of this type of computer-aided design (CAD) tool [5]–[9]. Additionally, this type of CAD tools can design various type of analog circuits and develop high-performance and variation-tolerant circuits. Different techniques at the schematic level for automatic analog circuit design are presented in different literature that can be classified as: knowledge-based and optimization-based. The designer of analog circuit produce synthesis rules according to their expertise and experience in the area of analog design in the knowledge-based technique. Design solution is obtained by incorporating these rules with algorithm [10]–[14]. This method is complex, lengthy, and applicable to only

some of the analog circuit topologies. The optimization process incorporates greedy search algorithm which finds the results towards a solution [10], [15]–[21]. This technique is very much result oriented and gives proper desired results. Recent research is concentrated to automate the analog circuit design which results in a novel metahuristic algorithms are explored in the area of analog circuit design. In this work, an attempt is made to find the optimum design of a differential amplifier circuit using different.

2. AUTOMATED CIRCUIT DESIGN METHOD

This paper is committed to exploring the evolutionary algorithms (EA) for the automated analog circuit design of complementary metal oxide semiconductor (CMOS) based analog circuits. The main issue is to determine the best dimensions of transistor, that is the goal of a CAD tool used to design analog circuit. Generally, it is denoted as an automated analog circuit sizing. According to the desired specifications, the relation between different circuit parameters i.e. channel length (L) and channel width (W) of the metal oxide semiconductor (MOS) transistors should be maintained during the optimization process of analog circuits design. The structure of the automated circuit design is shown in Figure 1. From the results obtained through the circuit simulator, the cost function is obtained by (1) [22]:

$$CostFunction = \sqrt{\sum_{j=1}^{D}\left(\frac{Specification_{desired}-Specification_{simulated}}{Specification_{desired}}\right)_j^2} \quad (1)$$

In (1) desired specifications mentioned by D. Equal weightage is allocated to all the desired specifications by the root mean square error. As a result, the optimizer make an effort to satisfy all the required specifications with equal importance. Then, termination criteria is checked. For the termination of algorithm decided by minimum value of cost function or a maximum number of iterations.

In the present design, the least cost function value is taken 1e-6 and the utmost iterations number is taken as 100. A new design parameters set will be created by EA when it fails to reach the termination criteria. To obtain the required value of the cost funcion that is the major task of this system. This system will perform this task for the given circuit within maximum iteration limit. The optimizer performance is extremely reliant on parameters of the used optiomization algorithm, design parameters of the used circuit, number of the desired specifications, and search space of the design parameters [23].

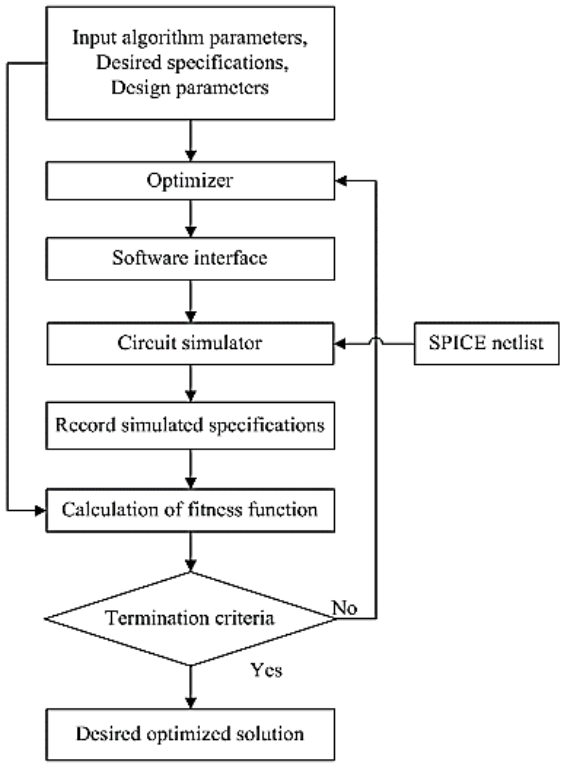

Figure 1. Flow diagram for automatic circuit design [23]

The effectiveness of the optimizer is very much reliant on algorithm parameters, different design parameters of a circuit, a number of the desired specifications and search space of the design parameters. In this work, the cuckoo search (CS), particle swarm optimization (PSO), differential evolution (DE), and hybrid chaotic serial particle swarm optimization (CSPSO) algorithms are tested by optimizing the differential amplifier (DA) for the given specifications independently. Table 1 gives the factors settings for the PSO, DE, CS, and hybrid CSPSO algorithms for the process of optimization. Automated simulation environment consists of simulator program with integrated circuit emphasis (SPICE) simulation environment and optimizer to optimize the differential circuit as an optimization problem to achieve desired specifications. The optimizer uses various optimization algorithms of DE, PSO, CS, and CSPSO to optimize design parameters like w, l for the targeted specifications. The result achieved by the algorithms is simulated by the simulating circuit in Ngspice circuit simulator. The desired specifications of differential amplifier and algorithm parameters are given as input.

Table 1. Values of different parameters of tested algorithms

Sr. No.	Factors of PSO algorithm	Factors of DE algorithm	Factors of CS algorithm	Factors of CSPSO algorithm
1	Number of particles (N)=30	Populations size (N)=30	Number of nests (N)=30	Number of nests (N)=30
2	C_1=1.49	CR=0.5	p_a=0.25	p_a=0.25
3	C_2=1.49	F=0.8	---	C_1=1.49
4	$V_{max} = x_{max}$	---	---	C_2=1.49
5	$V_{min} = x_{min}$	---	---	$V_{max} = 0.1 * x_{max}$
6	ω changes between 0.9 to 0.4 linearly with iterations	---	---	$V_{min} = 0.1 * x_{min}$
7	---	---	---	ω changes between 0.9 to 0.4 linearly with iterations

3. DIFFERENTIAL AMPLIFIER USING A CURRENT MIRROR LOAD

The differential amplifier using a current mirror load is shown as a circuit diagram in Figure 2. The theoretical as well as arithmetical analysis of this circuit is given in [24]–[26]. The value of load capacitor is chosen 0.5 pF for the optimization process of this circuit. ±1.8 V is selected as a supply for 0.18 µm CMOS technologies respectively.

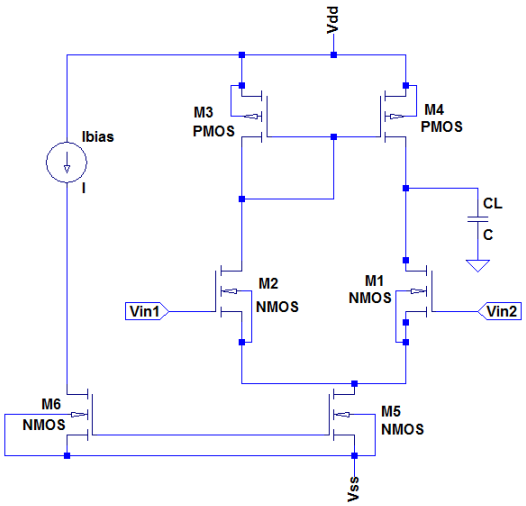

Figure 2. Differential amplifier using a current mirror load [21]

4. RESULTS AND ANALYSIS

Results obtained using different EAs in this work for the DA circuit using 0.18 µm CMOS technology are listed in Table 2. The results are the search space and design parameter values optimized. The specifications achieved through Ngspice simulator for obtained design parameters are listed in Table 3. These specifications found by utilizing different EAs for the given circuit and the preferred specifications. This work is tested for the designing DA circuit with 0.18 µm CMOS technology by the different algorithms like

DE, PSO, CS, and hybrid CSPSO algorithms. For the given circuit, the number of required specifications is 12 which are PM, A_v, UGB, FSR, +ve PSSR, -ve RSR, total MOS transistor area (TTA), total integrated input-referred noise (N_{int}) over the specific frequency range 1 Hz to 100 kHz, PSSR, CMRR, P_{diss}, and input-referred noise spectral density (N_{in}) @10 kHz.

Required specifications and optimized specifications during the simulation process using the different EAs for this circuit with 0.18 µm CMOS technology are recorded in Table 3. For this circuit using 0.18 µm CMOS technology, total MOS TTA of 203.36 µm^2 and 248.95 µm^2 are obtained for CS and CSPSO algorithms for the desired targeted specifications. The power dissipation (P_{diss}) and TTA achieved by the CSPSO and CS algorithms are lower as in contrast to those obtained through the PSO and DE algorithms. The CS algorithm obtained all the targeted specifications with low P_{diss} i.e. 29.04 µW and the least TTA i.e. 203.36 µm^2 compared to those achieved through the PSO and DE algorithms. Singh *et al.* [27] worked on analogous circuit by using PSO algorithm with aging leader and challengers (ALCPSO) algorithm in the CMOS technology. Table 3 shows the result for comparison of the performance. It can be seen from the results that even though considering additional specification sour methodology can still fulfil the objective function of the given design problem.

Table 2. Search space and optimized parameters by different EAs for DA in 0.18 µm CMOS technology

Sr. No.	Design parameters	Range of design parameters	Achieved values				
			PSO	DE	CS	CSPSO	[27]
1	$W_1 = W_2$(µm)	3.5 to 30	30.00	30.00	22.63	21.26	6.38
2	$W_3 = W_4$(µm)	3.5 to 30	12.79	11.82	3.50	4.57	6.24
3	$W_5 = W_6$ (µm)	3.5 to 30	28.39	30.00	7.30	10.08	2.8
4	I_{bias}(µA)	3.5 to 30	10.00	5.86	5.81	5.52	---

Table 3. Desired specifications and simulation results by different EAs for DA in 0.18 µm CMOS technology

Sr. No.	Specifications	Expected value	Obtained Specifications				
			PSO	DE	CS	CSPSO	[27]
1	A_v(dB)	>40	40.12	40.05	40.48	40.59	42.15
2	UGB (MHz)	>10	23.76	16.68	17.72	25.23	2.48
3	PM (°)	>45	46.22	47.70	53.31	47.68	60.38
4	+ve PSSR (dB)	>40	40.85	40.75	41.20	41.31	--
5	-ve PSSR (dB)	>70	70.82	70.25	70.01	70.11	--
6	RSR (V/µs)	>10	25.92	16.52	14.36	21.94	12.32
7	FSR (V/µs)	>10	17.62	11.08	11.46	17.16	--
8	CMRR (dB)	>70	68.79	70.06	70.30	70.06	--
9	P_{diss}(µW)	<1,000	53.69	32.11	**29.04**	**44.34**	--
10	N_{in}(nV/$\sqrt{Hz}$) @ 10 kHz	<50	128	182	22.62	79	21.26
11	N_{int}(μV_{rms}) (1 Hz–100 kHz)	<50	1.83	1.88	7.20	1.66	--
12	TTA (µm^2)	<400	379.00	376.71	**203.36**	**248.95**	87.35

In Table 4, the performance of the PSO, CS, DE, and hybrid CSPSO algorithms for the optimization of the circuit in 0.18 µm CMOS technology for ten independent runs are given. The CS, DE, and hybrid CSPSO algorithms achieved ten out of ten runs to get every desired specification throughout the process of optimization of the given circuit, while the PSO algorithm could succeed for only one time. The CS algorithm in contrast to the PSO, DE, and CSPSO algorithms achived optimization process with average number of iterations $(Iter_{avg})$ for 10 individual runs for this circuit.

Table 4. Performance analysis for tested EAs

Algorithm	$SD_{fitness}$	$Iter_{avg}$	FE_{avg}	S_{rate}	T_{sim} (s)
DE	0.0	14.10	**453**	10	**1019**
PSO	0.0074	90.1	3000	1	6027
CS	0.0	**11.4**	714	10	1317
CSPSO	0.0	15.2	1398	10	3076

Zero standard deviation of the cost function value is obtained by the DE, CSPSO, and CS algorithms, while standard deviation 0.0074 is obtained by the PSO algorithm. Thus, the CSPSO and CS algorithms do better than the PSO algorithm for this particular case. Figure 3 shows the convergence performance of the DE, CS, CSPSO, and PSO algorithms for the optimization of DA using 0.18 µm CMOS

technology. From the figure it can concluded that CS algorithm reaches faster to the desired fitness value in comparison to the DE, CSPSO, and PSO algorithm.

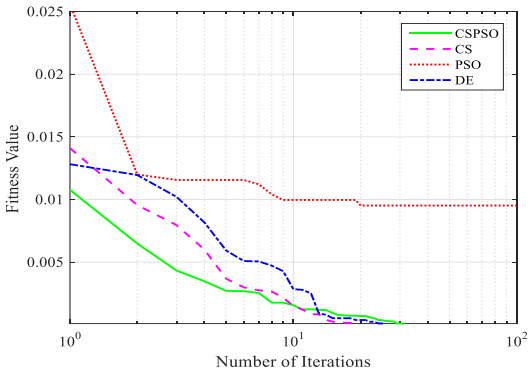

Figure 3. Convergence performance of different EAs

5. CONCLUSION

The problem to design an analog circuit is depending on number of targeted specifications as well as the different values of design parameters of a given circuit. In this work, the PSO algorithm has obtained fitness function value (SD_f) 5.1e-3 but not able to targeted standard deviation. Zero standard deviation is achieved by the CS, DE, and CSPSO algorithms but these algorithms are not able to achieve targeted fitness function values. From this work, we can conclude that CS, DE, and CSPSO algorithms give better performance as compared to the PSO algorithm. The CS and CSPSO algorithms attained desired specifications with low P_{diss} and the least TTA compared to those achieved through the PSO and DE algorithms.

REFERENCES

[1] S. L. Sabat, K. S. Kumar, and S. K. Udgata, "Differential evolution and swarm intelligence techniques for analog circuit synthesis," *2009 World Congress on Nature and Biologically Inspired Computing, NABIC 2009-Proceedings*, pp. 469–474, 2009, doi: 10.1109/NABIC.2009.5393356.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. China: McGraw-Hill, 2005.

[3] M. Barros, J. Guilherme, and N. Horta, *Analog circuits and systems optimization based on evolutionary computation techniques*. Warsaw, Poland: Springer, 2008. doi: 10.1007/978-3-642-12346-7.

[4] M. Kubař and J. Jakovenko, "A powerful optimization tool for analog integrated circuits design," *Radioengineering*, vol. 22, no. 3, pp. 921–931, 2013.

[5] S. N. Ahmadyan, *Validation and optimization of analog circuits using randomization serach algorihms*. Urbana, Illinois: University of Illinois, 2016.

[6] B. P. De, K. B. Maji, R. Kar, D. Mandal, and S. P. Ghoshal, "Design of Optimal CMOS Analog Amplifier Circuits Using a Hybrid Evolutionary Optimization Technique," *Journal of Circuits, Systems and Computers*, vol. 27, no. 2, pp. 1–23, 2018, doi: 10.1142/S0218126618500299.

[7] M. N. Sabry, H. Omran, and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelectronics Journal*, vol. 75, no. October 2017, pp. 87–96, 2018, doi: 10.1016/j.mejo.2018.02.002.

[8] A. Dendouga and S. Oussalah, "Telescopic op-amp optimization for mdac circuit design," *Electronics*, vol. 20, no. 2, pp. 55–61, 2016, doi: 10.7251/ELS1620055D.

[9] S. Asaithambi and M. Rajappa, "Swarm intelligence-based approach for optimal design of CMOS differential amplifier and comparator circuit using a hybrid salp swarm algorithm," *Review of Scientific Instruments*, vol. 89, no. 5, pp. 1–9, 2018, doi: 10.1063/1.5020999.

[10] G. Alpaydin, S. Balkir, and G. Dündar, "An evolutionary approach to automatic synthesis of high-performance analog integrated circuits," *IEEE Transactions on Evolutionary Computation*, vol. 7, no. 3, pp. 240–252, 2003, doi: 10.1109/TEVC.2003.808914.

[11] M. G. R. Degrauwe *et al.*, "IDAC: An Interactive Design Tool for Analog CMOS Circuits," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 1106–1116, Dec. 1987, doi: 10.1109/JSSC.1987.1052861.

[12] R. Harjani, R. A. Rutenbar, and L. Richard Carley, "OASYS: A Framework for Analog Circuit Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 12, pp. 1247–1266, Dec. 1989, doi: 10.1109/43.44506.

[13] B. J. Sheu, A. H. Fung, and Y. N. Lai, "A knowledge-based approach to analog IC design," *IEEE Transactions on Circuits and Systems*, vol. 35, no. 2, pp. 256–258, Feb. 1988, doi: 10.1109/31.1735.

[14] F. El-Turky and E. E. Perry, "BLADES: An Artificial Intelligence Approach to Analog Circuit Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 6, pp. 680–692, Jun. 1989, doi: 10.1109/43.31523.

[15] H. Y. Koh, C. H. Séquin, and P. R. Gray, "OPASYN: A Computer for CMOS Operational Amplifiers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 2, pp. 113–125, Feb. 1990, doi: 10.1109/43.46777.

[16] W. Nye, D. C. Riley, A. SangiovannI-Vincentelli, and A. L. Tits, "Delight. Spice: An Optimization-Based System for the Design of Integrated Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 7, no. 4, pp. 501–

519, Apr. 1988, doi: 10.1109/43.3185.
[17] F. Medeiro, F. V. Fernández, R. Domínguez-Castro, and A. Rodríguez-Vázquez, "A Statistical OptimizationBased Approach for Automated Sizing of Analog Cells," in *IEEE/ACM International Conference on Computer-Aided Design*, 2009, pp. 594–597. doi: 10.1109/9780470544310.ch13.
[18] B. Benhala, A. Ahaitouf, M. Fakhfakh, and A. Mechaqrane, "New Adaptation of the ACO Algorithm for the Analog Circuits Design Optimization," *IJCSI International Journal of Computer Science Issues*, vol. 9, no. 3, pp. 360–367, 2012
[19] Pankaj P. Prajapati and Mihir V. Shah, "Automatic Circuit Design of CMOS Miller OTA Using Cuckoo Search Algorithm," *International Journal of Applied Metaheuristic Computing (IJAMC)*, vol. 11, no. 1, pp. 36-44, 2020, doi: 10.4018/IJAMC.2020010103.
[20] P. P. Prajapati and M. V. Shah, "Automatic sizing of CMOS-based analogue circuits using Cuckoo search algorithm," *International Journal of Intelligent Systems Technologies and Applications*, vol. 19, no. 2, pp. 125–140, 2020, doi: 10.1504/IJISTA.2020.107217.
[21] P. P. Prajapati, A. J. Kshatriya, S. L. Bharvad, and A. B. Upadhyay, "Performance analysis of CMOS based analog circuit design with PVR variation," *Bulletin of Electrical Engineering and Informatics*, vol. 12, no. 1, pp. 141–148, 2023, doi: 10.11591/eei.v12i1.4357.
[22] R. A. Thakker, M. S. Baghini, and M. B. Patil, "Low-Power Low-Voltage Analog Circuit Design Using Hierarchical Particle Swarm Optimization," in *2009 22nd International Conference on VLSI Design*, Jan. 2009, pp. 427–432. doi: 10.1109/VLSI.Design.2009.14.
[23] P. P. Prajapati, "Computer aided CMOS based analog circuit design," Ph.D. thesis, Department of Electronics & Communication Engineering, Gujarat Technological University, Ahmedabad, India, 2019.
[24] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. India: Oxford University Press, 2013.
[25] R. A. Vural and T. Yildirim, "Analog circuit sizing via swarm intelligence," *AEU - International Journal of Electronics and Communications*, vol. 66, no. 9, pp. 732–740, 2012, doi: 10.1016/j.aeue.2012.01.003.
[26] S. Mallick, R. Kar, S. P. Ghoshal, and D. Mandal, "Optimal sizing and design of CMOS analogue amplifier circuits using craziness-based particle swarm optimization," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 29, no. 5, pp. 943–966, 2016, doi: 10.1002/jnm.2155.
[27] C. L. Singh, C. Anandini, and A. J. Gogoi, "Automated sizing of low-noise CMOS analog amplifier using ALCPSO optimization algorithm," *Journal of Information and Optimization Sciences*, vol. 39, no. 1, pp. 99–111, 2017, doi: 10.1080/02522667.2017.1380408.

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