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FPGA implementation of DTCWT architecture's high-speed DA structure for OFDM-based transceiver with CS

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ABSTRACT

Communication systems at millimeter-wave (mm-wave) frequencies with high propagation losses use radio frequency (RF) budget analysis. RF system gains and losses ensure the receiver can recover the broadcast signal. Modern communication systems use compressive sensing (CS) and discrete wavelet transform (DWT). Hardware implementation is hard. Field-programmable gate arrays (FPGA) adaptability, configurability, and processing speed make them popular. More mm-wave transceivers use FPGAs and advanced signal processing. FPGA-based mm-wave transceivers use compressed sensing and dual-tree complex wavelet transform (DTCWT). RF budget analysis recovers receiver signals. Energy and data efficiency transceivers have baseband processors, transmitters, and receivers. RF-to-mm-wave transmitter. Receiver demodulation and baseband conversion. CS and DTCWT processing modules boost baseband signal processing 5 Gbps Xilinx virtex-6 FPGAs. The system retrieves the signal while conserving power, according to simulations and testing. This study found that FPGA-based mm-wave transceivers can use advanced signal processing in future high-speed communication systems.

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1. INTRODUCTION

Radio frequency (RF) budget analysis is a necessary stage in the design process for communication systems [1], particularly when those systems will be operating at millimeter-wave (mm-wave) frequencies and will be subject to significant propagation losses. In order to guarantee the correct recovery of broadcast signals, it is essential to conduct an analysis of the gains and losses that occur inside the RF system [2]. Because of their versatility, setup flexibility, and rapid processing speeds, field-programmable gate arrays (FPGAs) [3] have grown increasingly popular in recent years. There may be challenges involved in the hardware implementation of such systems [4]. Recent advancements in the field of mm-wave communication systems have significantly contributed to the industry in recent years. When combined with innovative signal processing techniques, FPGA-based mm-wave transceivers are gaining a significant amount of traction in the market [5]. The use of FPGAs provides a flexible and changeable hardware implementation, which makes effective signal processing and adaptability to system needs easier to achieve. The solution that we have given comes with a few advantages. Researchers and engineers have been actively studying creative techniques to address the challenges posed by mm-wave frequencies in order to meet the increasing need for high-speed and dependable wireless communication [6]. The use of cutting-edge technology such as discrete wavelet transform (DWT) [7] is essential to the success of today's communication networks in overcoming

the challenges. By simulating and testing our suggested system using a Xilinx virtex-6 FPGA, we are able to recover signals at a data rate of 5 Gbps, proving that it is effective [8]. The dual-tree complex wavelet transform (DTCWT), is an adaptable piece of technology that may be utilised in a wide number of ways inside wireless communication systems by Ribeiro *et al*. [9]. In the parts that follow, the FPGA-based mm-wave transceiver that was presented is investigated in great detail. Topics covered include the system architecture, various signal processing approaches, and performance testing. The results of the experiments show that the combined compressive sensing (CS) and DTCWT approach is effective for dependable signal recovery while using a low amount of electricity [10], [11]. CS and DTCWT processing modules nested within an FPGA-based mm-wave transceiver are two solutions that we recommend [12] for resolving the challenges at hand. With the addition of DTCWT processing modules, the system's capability to decode and process signals with sophisticated structures is improved, which enables more accurate and efficient baseband processing. In summary, the integration of cutting-edge technologies such as DTCWT and CS into FPGA-based mm-wave transceivers and wireless network-on-chips (WiNoC) offers promising solutions to overcome the challenges of high-frequency communication and on-chip data transfer. These advancements pave the way for the development of high-speed, reliable, and energy-efficient communication systems, catering to the increasing demands of modern wireless communication and many-core architectures [13], [14].

2. LITERATURE SURVEY

Recent research works have shown a growing interest in RF budget analysis and FPGA implementation of mm-wave supported transceivers with CS and DTCWT for wireless communication systems. Researchers [15] and [16] designed and implemented an FPGA-based mm-wave transceiver for 5G mobile communications. They utilized CS to reduce the number of samples needed to retrieve the transmitted signal, resulting in lower computing complexity and hardware requirements. Wei *et al*. [17] presented an FPGA-based 60 GHz mm-wave communication system employing low density parity check (LDPC) and CS for reliable communication. Their approach achieved excellent throughput with reduced power consumption compared to conventional systems. Cheng *et al*. [18] proposed an FPGA implementation of an orthogonal frequency division multiplexing (OFDM)-based mm-wave transceiver, incorporating CS to minimize the sample rate required for reliable communication. This approach demonstrated high data rates with improved hardware and power efficiency. The hierarchical mm-wave network-on-chip (mmWNoC) [19] and mmWNoC are two complementary metal-oxide-semiconductor (CMOS-compatible) WiNoC modules commonly used in network-on-chip (NoC) implementations. Energy efficiency is a critical concern in WiNoC design, and researchers have explored various techniques to reduce power consumption in transceivers. Deb *et al*. [20] proposed a wireless NoC architecture with mm-wave interconnects that demonstrated significant energy savings compared to traditional wired interconnects. They achieved this by using low-power CMOS-compatible transceivers with efficient power management strategies. Optimization methods have also been explored for locating NoC wireless interface sites.

WiNoCs operate in the sub-THz, mm-wave, THz frequency ranges [21], and zigzag antennas [22] have been identified as the best WiNoC antenna for space-efficient hardware implementation. Amplitude shift keying-on-off keying (ASK-OOK) is widely used in WiNoCs but consumes more energy than quadrature amplitude modulation (QAM) [23]. CMOS-based transceiver modules with OOK designs have been demonstrated with 18 GB/s data throughput at 60 GHz and low size and power overheads [24]. However, channel noise and low spectral efficiency can degrade performance [25]. To meet the ever-growing demands for high data rates in WiNoCs, researchers have explored multi-channel transceiver designs. Yu *et al*. [26] presented an architecture and design for a multi-channel mmWNoC using FPGA [27], demonstrating improved data throughput by utilizing multiple channels for parallel data transmission. WiNoCs employing code division multiple access (CDMA) with Walsh codes can achieve high data rates, generating 12 Tbps using a 256-core architecture [28]. To fulfill current technology parameters, high-performance central processing units are required, and transceiver module design plays a critical role in meeting these demands. With the increasing adoption of WiNoCs, security becomes a crucial aspect, and researchers have investigated secure communication techniques for WiNoC transceivers. Reviewed soft computing-based CS techniques in signal processing, which have potential applications in enhancing security by reducing vulnerability to signal interception. A WiNoC's on-chip transceiver module using OFDM can achieve data rates of 195.32 GB/s with channels in the mm-wave band [29]. Researchers have explored the use of a cyclic prefix and a 256-point fast fourier transform (FFT) module to shorten the modulation process. A DWT-based OFDM design improved bit error rate (BER) and inter-symbol interference (ISI). However, OFDM-based transceiver modules cannot employ DWT due to its shift variance. Innovative research replaces DWT with CS integrated DTCWT for modulation and demodulation in the WiNoC transceiver system [30]. The

integration of CS before transmission saves power while achieving the required data rate within a small area [31].

3. ORTHOGONAL MODULATION USING CS-DTCWT

Signals with sparse representation [32], in some bases, can be compressed and recovered using the technique of "CS." It is used to improve speech because of the restitution of sparse signals. The steps for CS based speech augmentation are as follows: sparse representation conversion creates a sensing matrix. Signal acquisition and reconstruction A hard cut replaces irrelevant coefficients with 0 after projecting the wavelet basis onto the non-sparse signal. The spare vector coefficients are multiplied by the random Gaussian-sensing matrix [33]. To rebuild the voice signal, optimization functions are used. Later, the original signal is recovered by the inverse method. Figure 1 presents the OFDM modulation block diagram that is designed for the generation of a 16-channel subcarrier using a three-stage inverse DTCWT structure. The input symbols X0 to X15 are modulated into the OFDM signal X(n). In every stage of processing, the filter coefficients La, Lb, Ha, and Hb are used for data processing. The intermediate filter outputs are represented as C1n and C2n for the first stage and second stages, respectively. In (1) represents the OFDM modulated data in every stage:

$$C1n = Xn + 0(z2)\, G0a\,(z) + Xn + 2(z2)\, G1a\,(z), n = 0, 1, 2, 3, \ldots, 15 \quad (1a)$$

$$C2n = Cn + 0(z2)\, G0a\,(z) + Cn + 2(z2)\, G1a\,(z), n = 0, 1, 2, 3, \ldots, 15 \quad (1b)$$

$$X(n) = ½\,\{C20(z2)\, G0a(z) + C21(z2)\, G1a(z)\} + ½\,\{C22(z2)\, G0b(z) + C23(z2)\, G1b(z)\} \quad (1c)$$

Subband coding generates the OFDM signal x(n) with filter coefficients at each level. DTCWT modulates and demodulates OFDM in Figure 1. The three-stage structure demodulates x(n) into 16 subcarriers using 10-tap filter coefficients. To add sparsity, W, jo, and k coefficient values below T are set to 0. A transmitter-receiver-known Gaussian random matrix contains it. Figure 1 shows a suggested DTCWT and inverse DTCWT OFDM transceiver. Encoder-decoder, OFDM modulator-demodulator, and RF frontend make up the transceiver model. QAM or quadrature phase shift keying **(**QPSK) modulators encode data bits into symbols for improved data speeds and spectrum efficiency. The N-stage synthesis filter bank structure orthogonally modulates encoded symbols using the inverse DTCWT model. Parallel-to-serial converters serialize modulated data. The digital upconverter converts modulated data into an mm-wave signal (by the carrier signal of frequency f0), and the power amplifier amplifies and transmits the analog data through the antenna. A low-noise amplifier (LNA) and digital down converter amplify the receiving signal without noise and convert the mm-wave signal to baseband data, respectively [34]. The serial-to-parallel converter buffers data for DTCWT processing. The N-stage analysis filter bank structure demultiplexes orthogonally, and the QAM or QPSK demodulator demodulates real and imaginary symbols to generate message data.

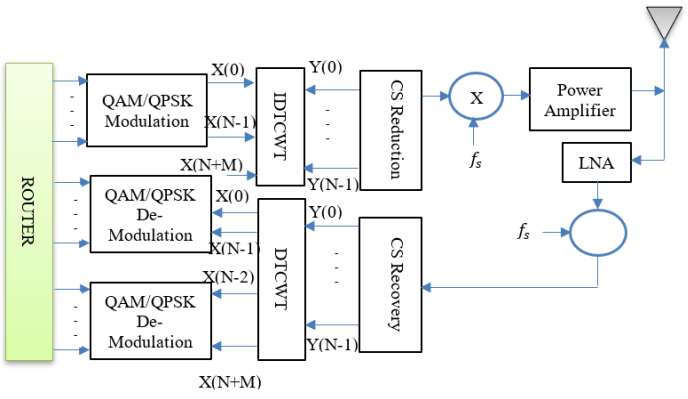


Figure 1. OFDM transceiver with inverse and forward DTCWT

The router module is the core of WNoC that directs the data within the system on chip (SoC). The advantages of the proposed OFDM transceiver are the increased data rate without the use of cyclic prefixes and improved spectral efficiency with the use of DTCWT-based OFDM modulation and demodulation. The power requirement of the RF front end is based on the chip area and the number of layers in the SoC.

3.1. Computation complexity of OFDM transceiver

Figure 1 shows a transceiver module with RF front end and baseband signal processing. Low-power RF front-end solutions are used with mm-wave technology and small communication distances. The transceiver's OFDM modulator/demodulator unit design is difficult. Forward and inverse DTCWT computation complexity limits the low-power implementation of DTCTW-based OFDM and N-stage subcarrier modulation. A 10-tap DTCWT filter with a minimum of four filters per stage generates 10 multipliers and 9 adders for each OFDM sample. The computation complexity of DTCWT implementation exponentially grows with an N-step analysis and synthesis filter bank structure, where each stage has twice as many filters. This work introduces a new architecture to simplify computation and optimize power dissipation.

3.2. Method

Dual tree complex wavelet transforms for FFT based OFDM model is captured considering different specifications. Figure 2 shows the flow of OFDM based FFT and DTCWT a random signal with 64 data bits is generated and QAM symbol mapped. The QAM symbols are processed by the OFDM structure designed using both FFT and DTCWT. The receiver module is designed to capture the signal from the channel and demodulate the symbols with different channel noise power.

After comparing the FFT and DTCWT BER plots for signal-to-noise ratios (SNRs) between -20 and -5 dB, it was determined that the MATLAB result for BER performance with different subcarriers was accurate. The BER plot of DTCWT-based OFDM, with a frequency range kept in the mm-wave spectrum appropriate for wireless NoC, is found to be superior to that of FFT-based OFDM. The DTCWT-based technique of OFDM was proven to produce superior BER and power spectral density (PSD) once the results were tested with different subcarrier lengths. Therefore, a low-power design strategy including distributed arithmetic (DA) architecture is developed in the next section.

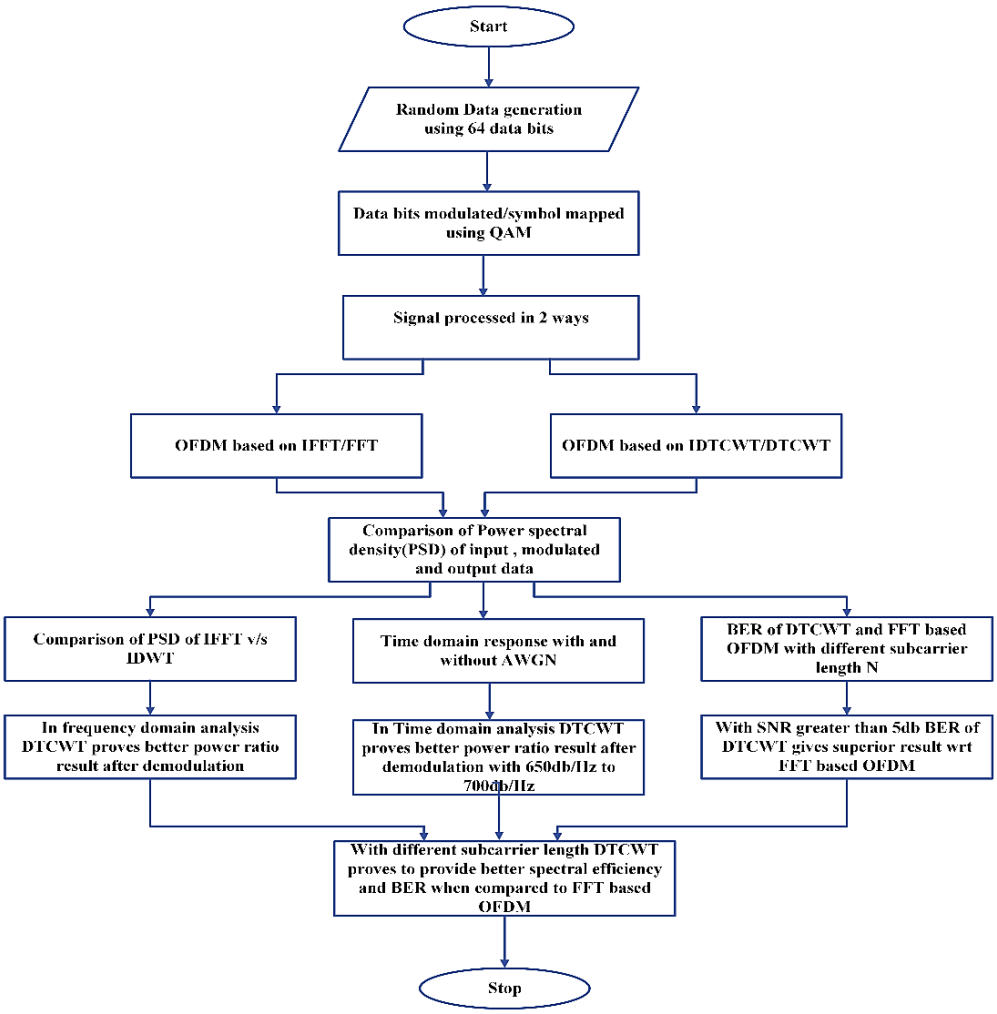


Figure 2. Simulation process of OFDM based on FFT and DTCWT

3.2.1. Design of low-power DTCWT architecture by high-speed distributed arithmetic architecture

Implementation of filter structure requires coefficients to be represented in binary numbers system. In order to minimize the number of binary bits for filter coefficient representation, the coefficients are multiplied by 256 and rounded off to the nearest integer. Representing the filter coefficients using integer representation requires a 9-bit binary word. The filter characteristics in terms of time domain and frequency domain responses are analyzed to choose the appropriate scaling factor to convert the fractional filter coefficients into inter-filter coefficients. Figure 3 presents the time domain response of the first stage filter of low pass and high pass of both real and imaginary trees. From the time domain response, it is observed that the imaginary filter is time delayed version of the real filter.

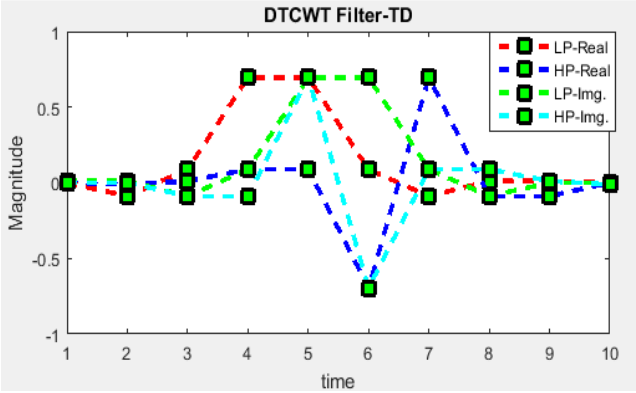


Figure 3. Time domain plot of DTCWT filters

Figures 4(a)-(d) shows the time domain response of DTCWT filters after scaling 64, 128, and 256. A scaling factor of 64 reduces filter coefficients substantially. Figure 3 shows the time-domain magnitude of all four filters. 256 scaling factor matches fractional filter coefficient zero crossings. From the frequency response, scaling by 64 and 256 retains the magnitude and phase response of fractional filters. Scaled low-pass and high-pass filter coefficients for real and imaginary tree structures. FPGA implementation of scaled DTCWT filters decomposes input images into several hierarchical subbands.

3.2.2. High-speed distributed arithmetic structure

Considering the convolution operation for a finite impulse response finite impulse response (FIR) filter, it is expressed as in (2). The input data Xk is the image pixels, and the filter coefficients are represented as Ak.

$$Y = \sum_{k=1}^{k} A_K X_K \tag{2}$$

The input samples represented in 2's complement representation considering 9-bit representation $\{b_{k0}, b_{k1}, b_{k2} \ldots . b_{k(n-1)}\}$, b_{k0} is the sign bit, and bk(n-1) is the least significant bit (LSB) and is represented as in (3):

$$X_K = -b_{k0} + \sum_{N=1}^{N-1} b_{kn} 2^{n-1} \tag{3}$$

Substituting in (3) into in (2), the filter expression is given as in (4):

$$Y = \sum_{K=1}^{K} A_k [-b_{k0} + \sum_{N=1}^{N-1} b_{kn} 2^{-n}] \tag{4}$$

Rearranging summation terms in (4) and representing two terms is given as in (5):

$$Y = \sum_{K=1}^{K} (b_{k0} A_k) + \sum_{k=1}^{k} \sum_{n=1}^{N-1} (A_K . b_{kn}) 2^{-n} \tag{5}$$

Expression (4) is expressed for the four filters of first stage DTCWT by replacing the filter coefficient Ak with the filter coefficients La, Ha, Lb, and Hb. In (6) presents the four filter expressions for the DTCWT filter with a 10-tap filter.

$$Y_{La} = -\sum_{K=1}^{10} b_{k0} h_{ak} + \sum_{k=1}^{10} [\sum_{n=1}^{N-1} (b_{kn} L_{ak}) 2^{-n}] \tag{6a}$$

$$Y_{Ha} = -\sum_{K=1}^{10} b_{k0} H_{ak} + \sum_{k=1}^{10} [\sum_{n=1}^{N-1} (b_{kn} H_{ak}) 2^{-n}] \tag{6b}$$

$$Y_{Lb} = -\sum_{K=1}^{10} b_{k0} h_{bk} + \sum_{k=1}^{10} [\sum_{n=1}^{N-1} (b_{kn} L_{bk}) 2^{-n}] \quad (6c)$$

$$Y_{Hb} = -\sum_{K=1}^{10} b_{k0} H_{bk} + \sum_{k=1}^{10} [\sum_{n=1}^{N-1} (b_{kn} H_{bk}) 2^{-n}] \quad (6d)$$

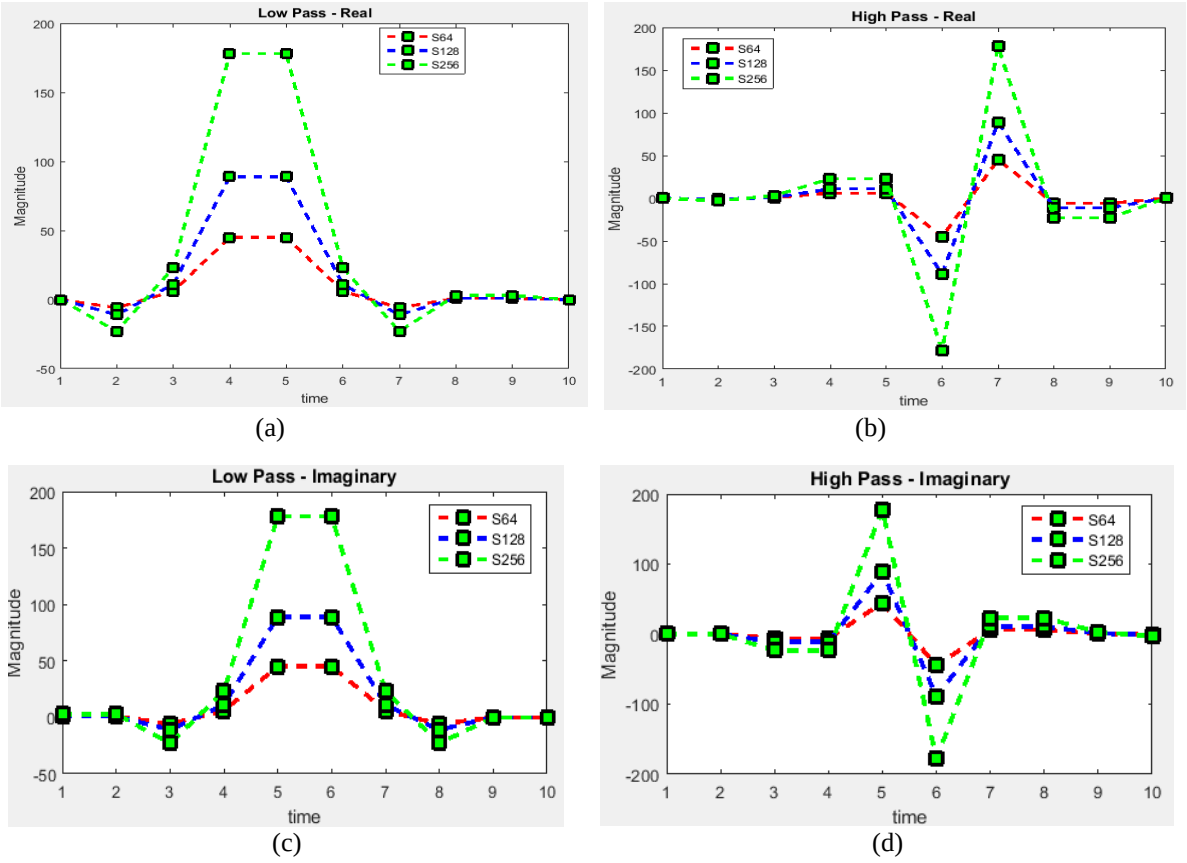


Figure 4. Time domain response of DTCWT filters with scaling; (a) simulated results of low pass filter, (b) simulated results of high pass filter, (c) simulated results of low pass for imaginary, and (d) simulated results of high pass for imaginary

Considering only the second term and expanding in (6a) by substituting the filter coefficients (7) is obtained.

$$Y_{La} = \sum_{K=0}^{10} \sum_{n=1}^{N-1} [(L_{ak.} b_{kn}) 2^{-n}] \quad (7)$$

Splitting in (7) into two terms as in (8), a split DA structure is designed.

$$Y_{La} = \sum_{K=0}^{4} \sum_{n=1}^{N-1} [(L_{ak.} b_{kn}) 2^{-n}] + \sum_{K=5}^{9} \sum_{n=1}^{N-1} [(L_{ak.} b_{kn}) 2^{-n}] \quad (8)$$

Considering in (8), which describes split DA logic, the input data represented as bkn is split into two parts of 4-bit each and is expressed mathematically as in (9).

$$Y_{La} = \begin{pmatrix} \sum_{K=0}^{4} \sum_{n=1}^{4} [(L_{ak.} b_{kn}) 2^{-n}] + \sum_{K=0}^{4} \sum_{n=5}^{8} [(L_{ak.} b_{kn}) 2^{-n}]) + \\ (\sum_{K=5}^{9} \sum_{n=1}^{4} [(L_{ak.} b_{kn}) 2^{-n}] + \sum_{K=5}^{9} \sum_{n=5}^{8} [(L_{ak.} b_{kn}) 2^{-n}] \end{pmatrix} \quad (9)$$

From (9), removing the common factor of 25 from the second and fourth terms and setting the summation limits for n=1 to 4, in (10) is obtained. DA structure realizing in (10).

$$Y_{La} = \begin{pmatrix} \sum_{K=0}^{4} \sum_{n=1}^{4} ([(L_{ak.} b_{kn}) 2^{-n}] + 2^5 \sum_{K=0}^{4} \sum_{n=1}^{4} [(L_{ak.} b_{kn}) 2^{-n}]) + \\ (\sum_{K=5}^{9} \sum_{n=1}^{4} ([(L_{ak.} b_{kn}) 2^{-n}] + 2^5 \sum_{K=5}^{9} \sum_{n=1}^{4} [(L_{ak.} b_{kn}) 2^{-n}]) \end{pmatrix} \quad (10)$$

Table 1 compares hardware metrics for all four designs. Table 1 shows hardware metrics of DA logic proposed in this work. From the comparisons presented in Table 1, the high-speed DA logic is faster in

terms of latency and throughput. The throughput is 5 clocks between two successive outputs to be generated and the first output is generated after 15 clocks demonstrating improvement in latency. The memory bits required for realizing high-speed DA logic is 160 bits which is an 84.375% improvement compared with the direct DA method. The critical path is increased by the addition of three adder delays as compared with direct implementation. The advantage of the high-speed DA logic is area is optimized and throughput is improved minimizing latency which is one of the requirements for implementation of DTCWT architecture on FPGA.

Table 1. Hardware metrics comparison for DA

Parameters	Direct DA	Split DA	Reduced memory DA	Improvised DA	High-speed DA
No. of look up tables (LUTs)	1	2	2	2	2
LUT size	1024	640	320	160	160
LUT arrangement	10×12	32×10 (2)	16×10 (2)	8×10 (2)	8×10 (2)
No. of adders	None	1	2	2	4
No. of accumulators	1	2	2	2	4
Critical path T	TLUT+TACC	TLUT+TACC+ TADD	T<TLUT+TACC+ TADD2+TADD2	T<TLUT+TACC +TADD2 +TADD2	TLUT+TADD1+ TADD2+TACC+ TADD3
Latency (clocks)	18	18	18	18	14
Throughput (clocks)	9	9	9	9	5

4. FPGA IMPLEMENTATION

This study models a high-speed DTCWT architecture in Verilog and verifies its functionality using random test vectors with 72% code coverage. The DTCWT and inverse DTCWT designs analyze and synthesize random data bits. To prove system logic, the output is compared to the input pattern. Xilinx ISE synthesizes and estimates area, power, and timing. Figure 5 shows the filter structure for the high speed DA. Figure 6(a) shows the filter bank synthesis network list for two outputs per clock. Inverse process synthesis network list in Figure 6(b).

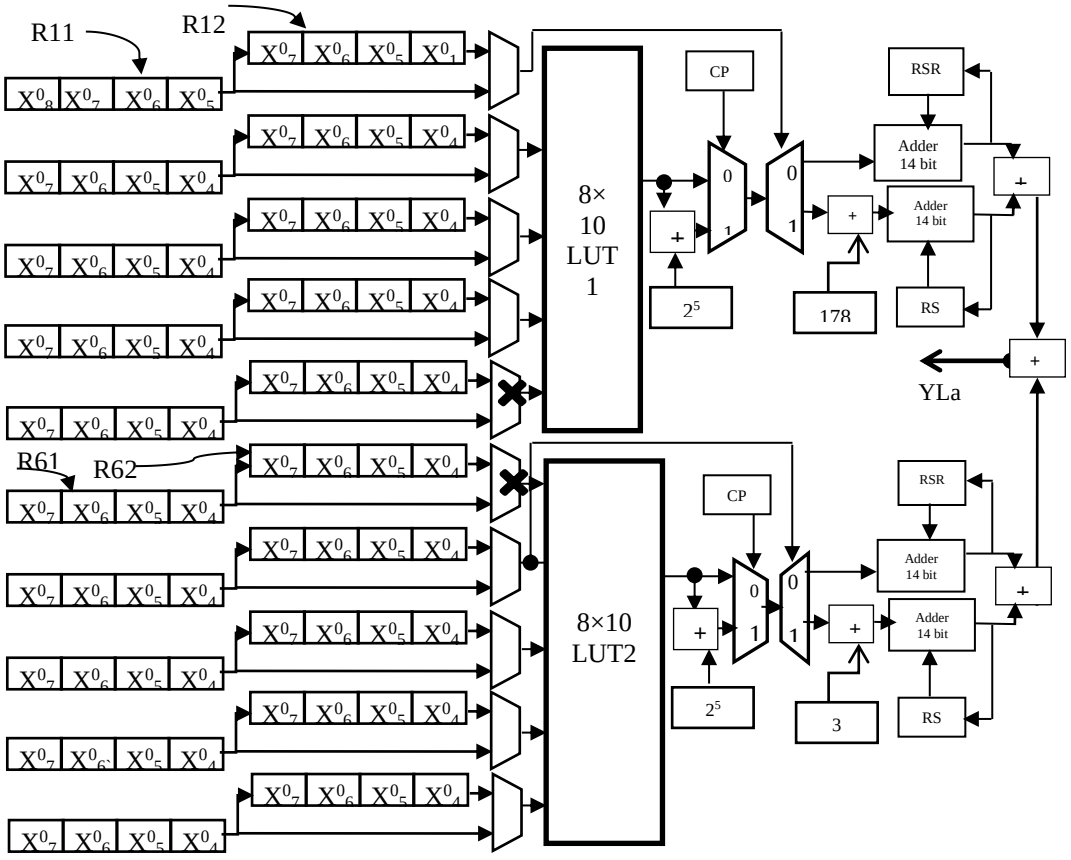
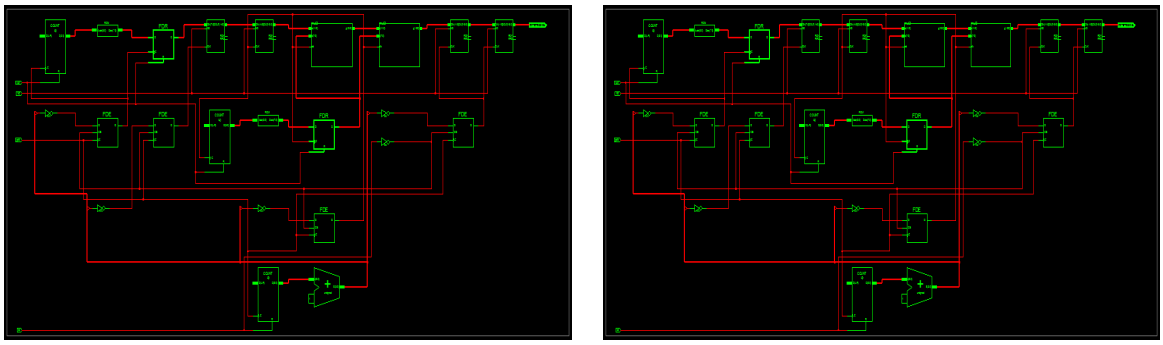


Figure 5. High speed reduced memory DA-based DTCWT filter structure for YLa



(a) (b)

Figure 6. Synthesis netlist real filter bank; (a) DTCWT filter and (b) inverse DTCWT filter

The FPGA implementation involves the following steps:

a. Hardware description: the implementation utilizes a Xilinx Virtex-6 FPGA with a specific clock frequency providing the required hardware resources for the DTCWT-based OFDM system.
b. DTCWT algorithms and wavelet filters: the DTCWT algorithms with filter bank synthesis which ensures efficient signal processing.
c. OFDM symbol generation: the DTCWT output is used to generate OFDM symbols, which are further modulated using M-QAM modulation.
d. Channel model: to simulate real-world communication conditions, a channel model is incorporated, considering noise and fading impairments.
e. Data processing steps: the demodulation of received OFDM symbols involves QAM demodulation and reconstruction of the original data using the inverse DTCWT.
f. FPGA implementation optimizations: pipelining and parallel processing techniques are employed in the FPGA design to achieve high-speed processing and efficient resource utilization.
g. Performance evaluation metrics: the performance is evaluated using BER and SNR as key metrics.
h. Power analysis: the power analysis demonstrates the FPGA-based system's low-power operation, ensuring energy-efficient communication.
i. Real-time testing and system integration: the FPGA-based DTCWT-based OFDM modulator and demodulator are validated in practical data transmission and reception scenarios, ensuring real-time functionality and system integration.

Figure 7 presents the power report for the DTCWT-inverse DTCWT pair for the real filter bank. The design is optimized for 40.99 mW of quiescent power and 1.67 mW of dynamic power dissipation. The proposed design is implemented on a Spartan-6 FPGA and the resource utilization is computed from the synthesis report. Table 2 presents the direct implementation of DTCWT using the convolution method and the proposed method for the real filter pair and Table 3 presents the hardware requirements for the filter bank. The synthesis report shows that the proposed design operates at a high frequency of 396 megahertz (MHz) with fewer slice registers than a direct implementation. DTCWT filters [35], which comprise real and imaginary filters are also implemented on FPGA [36], and a synthesis report is evaluated. The synthesis report identifies and compares the slice registers, LUTs, power, and maximum frequency of operation data with references. From the results obtained, the proposed design is faster in data processing and also consumes less power as compared with the reference designs [37], [38].

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.00026 (W)	5	---	---
Logic	0.00004 (W)	758	3840	19.7
Signals	0.00115 (W)	1385	---	---
IOs	0.00022 (W)	21	173	12.1
Total Quiescent Power	**0.04099 (W)**			
Total Dynamic Power	**0.00167 (W)**			
Total Power	**0.04266 (W)**			
Junction Temp	**26.3 (degrees C)**			

Figure 7. Power dissipation of real DTCWT and inverse DTCWT filter pair

Table 2. DTCWT and inverse DTCWT filter pair resource utilization

FPGA parameters Spartan 6	Available resources	Direct implementation	Proposed DTCWT
Slice registers	69120	665	612
Slice flip-flops (FFs)	1384	733	546
Slice LUTs	69120	822	762
Bonded input/output block (IOBs)	640	44	56
Max. frequency		284 MHz	396 MHz

Table 3. Comparison of hardware requirements for DTCWT filter bank

Variable	Proposed	[7]	[35]
Number of slice registers	2086	4112	7482
Number of slices LUTs	3022	4091	7224
Total power (W)	0.98	1.71111	2.00207
Max. frequency (MHz)	322.11	289.12	212.67

5. RESULTS AND DISCUSSION

The ModelSim simulation results for two different test cases are shown in Figures 8 and 9. Input data with an operating frequency of 58 MHz is modulated using an inverse DTCWT modulator and upconverted to the 32.43 GHz frequency band for transmission. The DTCWT demodulator and the digital down converter demodulate the received signal to generate the 58 MHz data signal, which is captured in signal to generate the 58 MHz data signal, which is captured in the simulation results. The first signal is a 50-578 MHz message signal modulated by the inverse OFDM structure and multiplied by the carrier signal at 43.24 GHz. The received signal is downconverted and demodulated to generate the message signal in the frequency band of 50 MHz to 578 MHz. From the simulation results obtained, it is demonstrated that the DTCWT-based OFDM modulator and demodulator designed using a modified DA algorithm are functionally correct in performing OFDM. The DTCTW-inverse DTCWT pair can be used as an intellectual property (IP) module for N-stage subcarrier modulation.

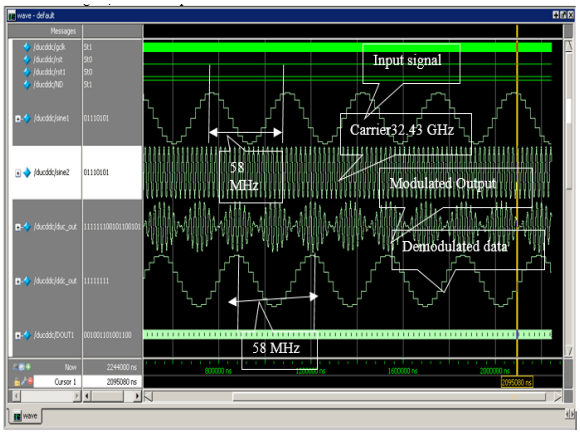


Figure 8. OFDM modulator (f0=32.43 GHz and 43.24 GHz)

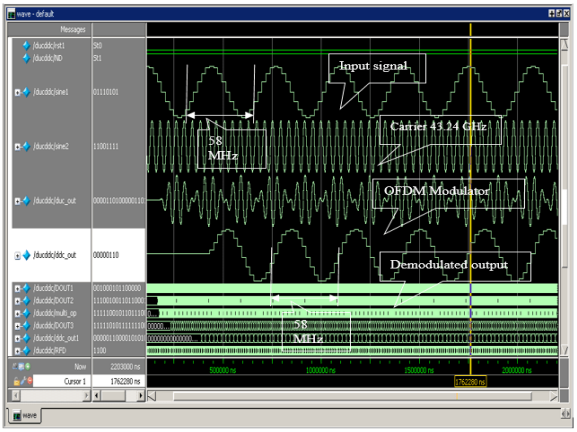


Figure 9. OFDM demodulator (f0=32.43 GHz and 43.24 GHz)

6. CONCLUSION

This work introduces the DTCWT to design, develop, and evaluate an OFDM modulator and demodulator DTCWT. We evaluated the method's area, power, and timing. Our research shows major gains over conventional methods. Compared to split logic, we reduced LUT memory by 75%. This memory decrease optimizes system area and power. We also saw a 22% latency improvement and a 44% throughput boost, showing signal processing efficiency and speed. We pipelined the forward and inverse DTCWT to increase data decomposition throughput. This architecture increased data decomposition throughput by 50%, increasing system efficiency. This study's OFDM-based architecture promises low-power, high-speed transceivers. We showed that DTCWT can boost communication speed and reduce power usage. Our research shows that DTCWT-based communication applications are feasible and effective. Our study introduces the DTCWT-based OFDM modulator and demodulator design and implementation. This method

significantly improves area, power, timing, latency, and throughput. These findings promote low-power, high-speed communication systems and inform future studies.

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