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A new topology of non-isolated AC-DC quadratic boost converter with enhanced power traits

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ABSTRACT

A novel AC-DC quadratic boost converter (QBC) topology is presented in this paper which can provide higher power factor (PF), lower total harmonic distortion (THD) and higher voltage when compared to a conventional AC-DC boost convertero This is achieved by using additional switched capacitor and switched inductor in the power processing stage. The presented converter is analyzed theoretically, and a voltage gain equation is derived. A simulation model is created to evaluate the converter performance under various duty cycles, switching frequency, and changing output load. The input PF, THD, and voltage gain of the simulated model were compared with conventional converter to determine the validity of the suggested converter circuit. The results show that the efficiency, PF, THD and voltage gain value reaches approximately 97.9%, 0.98, 16.14, and 2.83 respectively at a duty cycle of 50% with fixed output load of 100 Ω. A dual loop voltage and current controller is also arrayed with the proposed circuit which allows further enhancement in PF (0.997) and THD (7.45%). This converter can be a suitable option for systems where isolation is not necessary but high PF, high voltage gain and low THD are required.

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1. INTRODUCTION

Conversion between various voltage levels and providing a controlled flow of electrical power to the loads are accomplished by power electronic converters. Modern power electronic converter allows efficient power conversion due to the use of highly optimized power semiconductor devices and advanced control techniques. However, when a power converter draws discontinuous input current from AC mains, it can cause undesired effects such as low PF, high total harmonic distortion (THD) and high voltage and current stress on circuit components. This effect is mostly observed with non-linear loads, conventional AC-DC converters with large capacitive elements after rectification, and power converters with circuit topologies such that their input current is discontinuous due to the nature of their working principle. Low power factor (PF), high THD, and device stress can lead to significant problems such as heating of components, distortion of voltage, and low efficiency due to power loss [1]. Different AC-DC converters are presented in the literature to address these concerns. There are various AC-DC converters that provide voltage conversion as well as rectification. In line frequency AC-DC converters, a transformer is used for voltage conversion at the first stage and a rectifier with a filter at the second stage. In a typical high-frequency AC-DC converter, the primary stage is a full-bridge rectifier, and the later is a DC-DC converter operated by high frequency PWM pulses for voltage regulation. Typically, a boost converter is utilized in applications that require a higher

voltage gain. The traditional boost circuits have need of a very high duty ratio to achieve considerable voltage boosting, which stresses the components. In addition, the boosting capability of a traditional DC-DC boost converter is inadequate for high voltage applications [2]–[4]. It is also not feasible for applications where a large amount of power is required because it only has two power devices to process power across the load. Additionally, it shows the negative effects of high voltage and current stress [5]–[7].

Recent years have seen a proliferation of topologies aimed at achieving greater voltage gain, such as the clamped-inductor [8], [9] and charge pump techniques [10]. These circuits demonstrate superior gain at moderate duty cycles when compared to traditional boost converters. The clamped inductor technique has been demonstrated to achieve high boost voltage at duty ratios of 50-60% [5], [11]. However, these topologies also exhibit peak voltage and current stress limitations. One method of achieving high output voltage gain is through cascading two Boost converters, also known as cascaded boost or quadratic boost converters (QBC) [12]. However, this approach is associated with an increased component count. An alternative approach is the utilization of a multiple stage cascaded Boost converter, but this method comes with the trade-offs of increased circuit complexity, lower efficiency, and higher cost. The primary objective in the power electronics domain is to design a circuit that strikes a balance between simplicity and high efficiency while achieving a significant voltage gain. One approach to achieve this goal is by utilizing a single switch converter, such as the QBC. As demonstrated in [13], a cascaded DC-DC boost converter was suggested for micro source appliances. This circuit employs a traditional boost converter in tandem with a Flyback converter, using a single switch to minimize complexity. This circuit can achieve a voltage boosting up to twenty times the input but with the trade-off of increased conduction loss. Similar topologies have been proposed in [14], [15]. An alternative solution, proposed in [16], is the quadratic buck-boost topology which combines a boost and cuk converter, resulting in a continuous output current.

There is quite a large number of published research work that deals with QBC with high voltage gain but most of these only focuses on the input and output voltage ratio without considering the associated drawbacks of using extra bulky inductors, a large number of additional diodes, capacitors, and complex circuit design which can reduce the overall efficiency and reliability of the circuit. The quality of the input current, THD, and PF of those converters in AC-DC applications are not addressed. An interleaved QBC was presented in [14] which uses a Dickson voltage multiplier stage to raise the O/P voltage and interleaving to improve input current. Although the voltage gain and input current ripple are improved, the usage of four inductors and two power switches at the DC-DC stage makes this solution bulkier and more expensive. Furthermore, voltage multiplier cells have limited output current capability, and high ripple voltage, and are sensitive to load variations due to limited voltage regulation. A dual switch cubic SEPIC converter was presented in [17] with extra high voltage gain but with similar shortcomings of having several extra inductors, capacitors, and power switches which causes the overall circuit to be costlier and inefficient. A quadratic boost DC-DC converter was demonstrated in [18] with reduced voltage stress but this requires the use of additional clamping circuits and extra coupled inductors which increases the overall complexity of the circuit, and it is only appropriate for low-power appliances as the efficiency starts to fall dramatically for output greater than 100 W. A high step-up QBC utilizing a single switch was presented in [17] which uses the switched capacitor technique to lift the average dc output voltage and a clamped capacitor is utilized to clamp the voltage spike across the switch. However, due to the use of several inductors and many capacitors, the power density of the circuit is reduced. Another novel topology of quadratic boost with low inductor current is presented in [19] which uses two separate inductors to share the current and two power switches. Even though a detailed analysis of the converter circuit was made, its input current, THD, PF, and performance on AC-DC converter application are missing. Zeta-based converter and diode-capacitor assisted modified boost converters are presented in [20], [21]. A hybrid zeta converter based on SC-SL structure is presented in which can provide high voltage gain, but this topology uses three inductors, three capacitors and five diodes in the DC-DC stage alone which increases parts count and also reduces the reliability of the circuit due to high voltage and current stress in power semiconductor switch [20]. The converter in [21] achieves greater boosting using dual networks of diode-capacitors but the circuit operation is complex due to increased number of components.

The switches used in power electronic converters are subject to significant voltage stress. Recent research has focused on developing topologies that can mitigate this issue, such as the quadratic single switch boost DC-DC converter shown in [22]. This circuit employs coupled-inductor and switched-capacitor techniques to achieve both a high voltage gain and an improvement in efficiency, however, it also exhibits a high switching loss. Other studies, such as the updated buck-boost converters presented in [23], have sought to address issues such as input current continuity, but these designs do not achieve the same level of voltage gain as the QBC. An alternative approach is the QBC with an order of five, proposed in [24], which combines a traditional QBC with an extra capacitor and diode to achieve additional voltage gain and higher efficiency at mid-duty cycles. However, this circuit also has notable drawbacks such as a slow starting

response and high stress on switches. Another solution is the double closed-loop boost converter simulated by the average state space method in [15], this converter has a quick dynamic response and low output voltage ripple. In this work, a new single-phase non-isolated QBC is proposed and simulated, using PSIM to evaluate key performance metrics such as input PF, THD of input current, efficiency, and voltage gain under varying duty cycles, loads, and frequencies. The simulated results show that the suggested converter exhibits superior performance in terms of THD, efficiency, and PF when compared to a traditional converter, both with and without feedback. The results indicate that the proposed quadratic AC-DC non-isolated boost converter shows an acceptable performance.

2. METHOD

There are several types of AC-DC converters which can be grouped as isolated or non-isolated, step-down, or step-up. Here we are working with non-isolated AC-DC boost converter which can be further classified into cascaded boost, SC-SL boost, interleaved boost, coupled inductor boost, or quadratic boost. Our topology of interest is the quadratic boost where we proposed a modified hybrid topology based on SC-SL structure. The new single-phase AC-DC modified quadratic boost SC-SL based topology is analyzed and its performance is contrasted with traditional converter topology. The method flowchart for this converter design and analysis is shown in Figure 1. In this research work several assumptions were made while designing and simulation of the circuit, and they are listed below:

a. All diodes are assumed to be ideal
b. All passive components are assumed to be purely reactive
c. MOSFET ON resistance ($R_{ds}(On)$) is assumed to be zero
d. No initial capacitor voltage is considered for simulation
e. Input sine wave DC offset is assumed to be null
f. In controller circuit the comparators voltage, (Vs+=30 V) and (Vs-=-30 V)

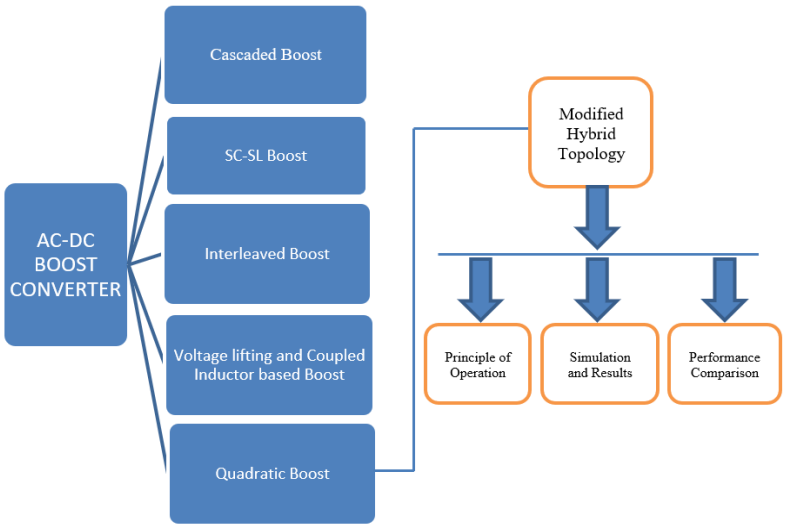

Figure 1. Method flowchart of the proposed system

3. PROPOSED CONVERTER: CIRCUIT DIAGRAMS AND OPERATION

The traditional topology of PFC AC-DC boost converter is shown in Figure 2 [25]. The suggested AC-DC QBC is demonstrated in Figure 3. The voltage gain equation of this converter maintains a quadratic function of the switching duty ratio (D). The proposed converter does not have any isolating component amid load and source. There are 3 inductors (Lin, L1, and L2), 4 capacitors (Cin, C1, C2, and Co), 6 diodes (D1 to D5 and D0), and a switch (SW1). The filter at the input side is constructed with inductor Lin along with capacitor Cin. The converter has L1 and L2 working as boost inductors and Co as filter capacitors at the load side. Resistor (Ro) represents the load of the converter.

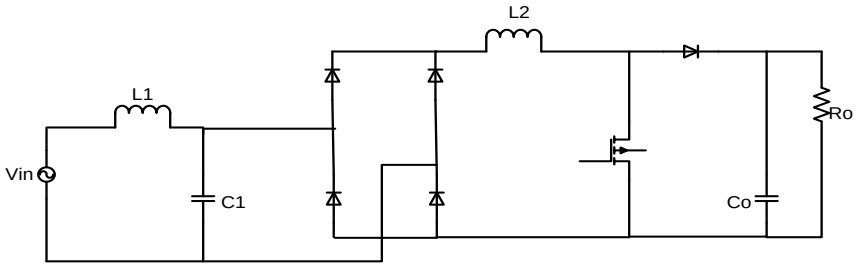

Figure 2. Conventional AC-DC boost converter with input filter [25]

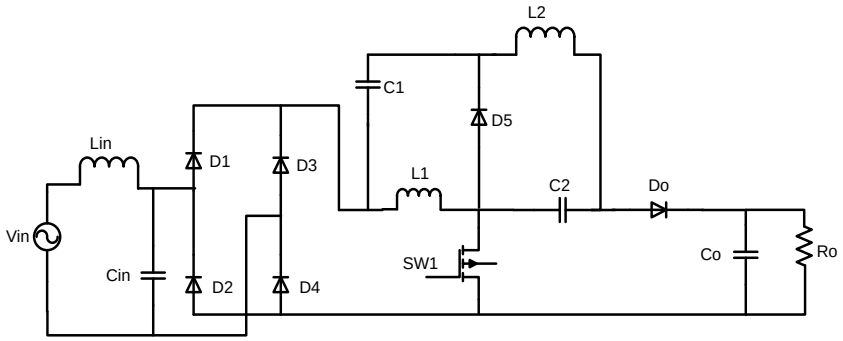

Figure 3. Proposed AC-DC QBC

There are four operating stages of the proposed converter. For one-half cycle of the input signal, there exist two modes depending upon the state of the switch. Similar modes exist for the other half cycle. The four operating modes of the prospective converter are provided in Figure 4. Figures 4(a) and (b) corresponds to mode 1 and 2. Figures 4(c) and (d) corresponds to mode 3 and 4.

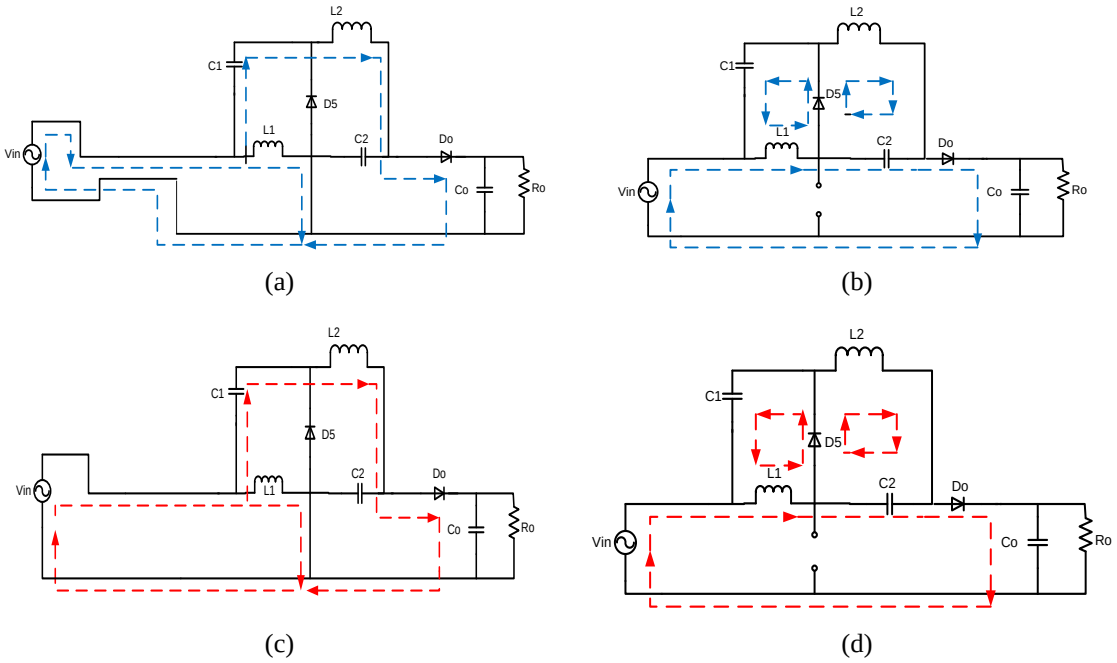

Figure 4. Four operating modes of the suggested converter; (a) mode 1: while SW1 is ON for (+ve) half cycle of input, (b) mode 2: while SW1 is OFF for (+ve) half cycle of input, (c) mode 3: while SW1 is ON for (-ve) half cycle of input, and (d) mode 4: while SW1 is OFF for (-ve) half cycle of input

Mode 1: while SW1 is ON throughout (+ve) half cycle of the input signal, L1, L2, and C1 gets charged from the source through two different paths.
Mode 2: SW1 is off for a positive cycle of input and L1 discharges through output capacitor Co as diode Do is forward biased. L1, C1, and L2, C2 form loops.
Mode 3: while SW1 is ON throughout (-ve) half cycle of input, same phenomenon occurs as mode 1. Just the input current is reversed through bridge rectifier.
Mode 4: SW1 is off for (-ve) half cycle of input and L1 discharges through Co, L1, C1, and L2, C2 form loops.

3.1. Ideal gain equation

The hybrid converter consists of two stages. A full-bridge rectifier tailed by a DC-DC converter. The rectified average voltage after the traditional diode bridge.

$$V_{o\_rec} = \frac{V_{in\_max}}{\pi} \int_0^{\pi} sin\theta d\theta = \frac{2V_{in\_max}}{\pi} \quad (1)$$

The second stage is an altered rendition of a DC-DC quadratic converter. After inductor volt-sec balance, its input-output voltage relation is given by (2):

$$V_o = \frac{1-D^2}{(1-D)^2} * V_{in} \quad (2)$$

Here D is duty ratio of the MOSFET. And, for the hybrid topology, the input to the DC-DC converter is given by $\frac{2V_{in\_max}}{\pi}$. So, the average O/P voltage of the hybrid converter is given by (3):

$$V_o = \frac{1-D^2}{(1-D)^2} * \frac{2V_{in\_max}}{\pi} \quad (3)$$

A graphical comparison has been made in Figure 5 between the theoretical O/P voltage from the gain equation and the simulated output voltage with varying duty cycles to prove the validity of the proposed AC-DC QBC circuit. It can be observed from Figure 5 that the simulated results are in close concession with theoretical results up to a duty cycle of 60% after which the simulated results give lower output voltage which might be due to the increasing non-linearities of the components at high input currents and high output voltage levels. Also, it is quite impractical for QBC to be operated at duty cycle values beyond 50% since the output voltage level reaches more than 600 V and causes high current stresses and voltage stresses in the power switches and other semiconductor components. Overall, the functionality of the proposed circuit is validated within the practical duty cycle range.

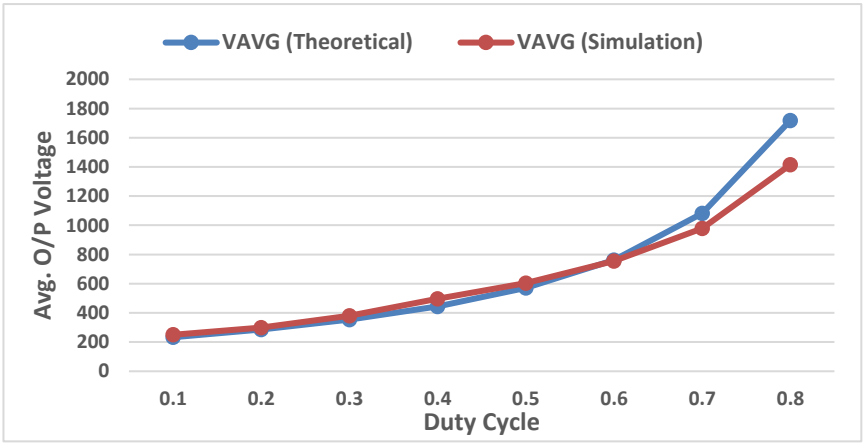

Figure 5. Comparison between theoretical output voltage and simulation output voltage

4. SIMULATED RESULTS AND PERFORMANCE ANALYSIS

Open-loop simulation of the proposed converter is carried out using PSIM. 300 volt peak AC supply with 50 Hz frequency is chosen as input for simulation. MOSFET is used as a switch. The values of different components for the circuit are Lin=1 mH, L1=L2=4 mH, Cin=1 µF, C1=C2=110 µF, and Co=20 µF.

R_0=100 Ω acts as the load of the converter. Table 1 illustrates the detailed performance of the QBC when the switching frequency is set at 10 kHz.

Table 1. Simulation outcomes of suggested converter for various duty cycle (D)

Duty cycle	Efficiency (%)	THD (%)	Input PF	Voltage gain
0.1	99.52	29.52	0.905	1.9
0.2	99.37	30.56	0.92	1.5
0.3	98.91	28.17	0.95	1.9
0.4	98.36	20.76	0.97	2.32
0.5	97.92	16.14	0.98	2.83
0.6	97.18	12.41	0.99	3.52
0.7	96.29	14.23	0.98	4.53
0.8	94.50	26.54	0.96	6.45
0.9	92.87	14.92	0.85	10.87

4.1. Performance study over duty cycle (D) change

The proposed and conventional converters both are simulated with the identical switching frequency of 10 kHz and a load of 100 Ω. The performance of both converters is analyzed under different duty cycle variations. The inductors and capacitors values for conventional circuits are L1=L2=1 mH, C1=1 µF, and C_O=20 µF. Figure 6(a) represents that; the input PF is higher in the case of the suggested converter in contrast with the traditional converter over D variation. The difference in PF is clearly visible as the highest PF the conventional converter can achieve is 0.93 whereas the suggested converter can provide a PF as high as 0.99, which is almost close to unity. As observed from Figure 6(b), the suggested topology has superior power conversion efficiency for lower duty ratios but for higher duty ratios, the conventional converter has the upper hand. THD of the input current is comparatively lower in the case of the proposed converter in contrast with the conventional converter over D variation as depicted in Figure 6(c). The suggested converter can maintain input current THD below 20%, for four separate duty cycles (duty cycle of 0.5, 0.6, 0.7, and 0.9) whereas the conventional converter can achieve below 20% THD for excessively high duty cycle (duty cycle of 0.9). As seen in Figure 6(d), the suggested topology gives a much larger boost voltage than the traditional one all through the D variation. The suggested circuit can provide voltage boosting up to 11 times whereas the conventional converter can provide maximum boosting up to 8.5 times.

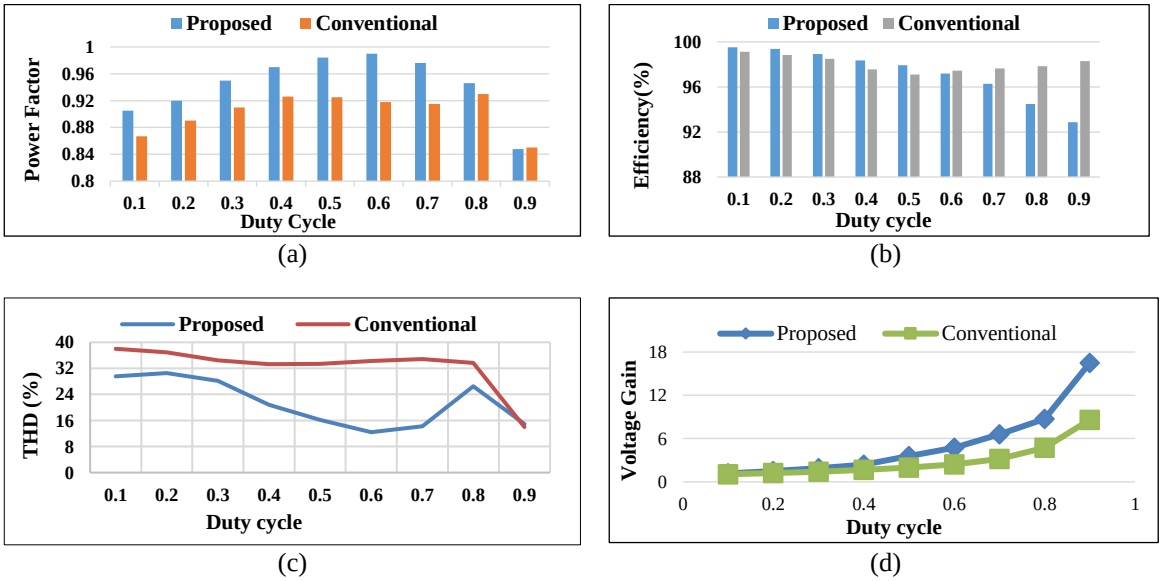

Figure 6. Graphical contrast of; (a) input PF, (b) efficiency (%), (c) THD (%), and (d) voltage gain amid suggested and traditional converter under D variation

4.2. Performance study under load resistance (Ro) variation

The proposed and conventional converter both are simulated with the same switching frequency of 10 kHz and the same D of 0.5. The performance of both converters is analyzed under load variation (50 Ω to

350 Ω). As seen in Figure 7(a), the input PF is higher in the case of the suggested converter correlated to the conventional converter for lower loads. The PF can rise to 0.99, which represents a near unity PF. For higher loads, the conventional converter has a better PF. From Figure 7(b) we can see that the proposed converter exhibits superior power conversion efficiency compared to the conventional one with load variation except for load of 50 Ω. With the increase in load, the difference in efficiency becomes more visible as the proposed converter can achieve efficiency as high as 98.5% whereas the conventional converter can provide a maximum level of efficiency of 95.8%. From the perspective of input current THD, the performance is better in the case of the proposed topology for lower amounts of loads but for higher amounts of loads the conventional converter has supremacy as observed from Figure 7(c). As seen in Figure 7(d), the suggested topology grants a higher boost voltage than the traditional one over the change of load. The proposed circuit provides voltage boosting above 3 times starting from a load of 150 Ω whereas the conventional one has this kind of boosting only for a high amount of load (350 Ω).

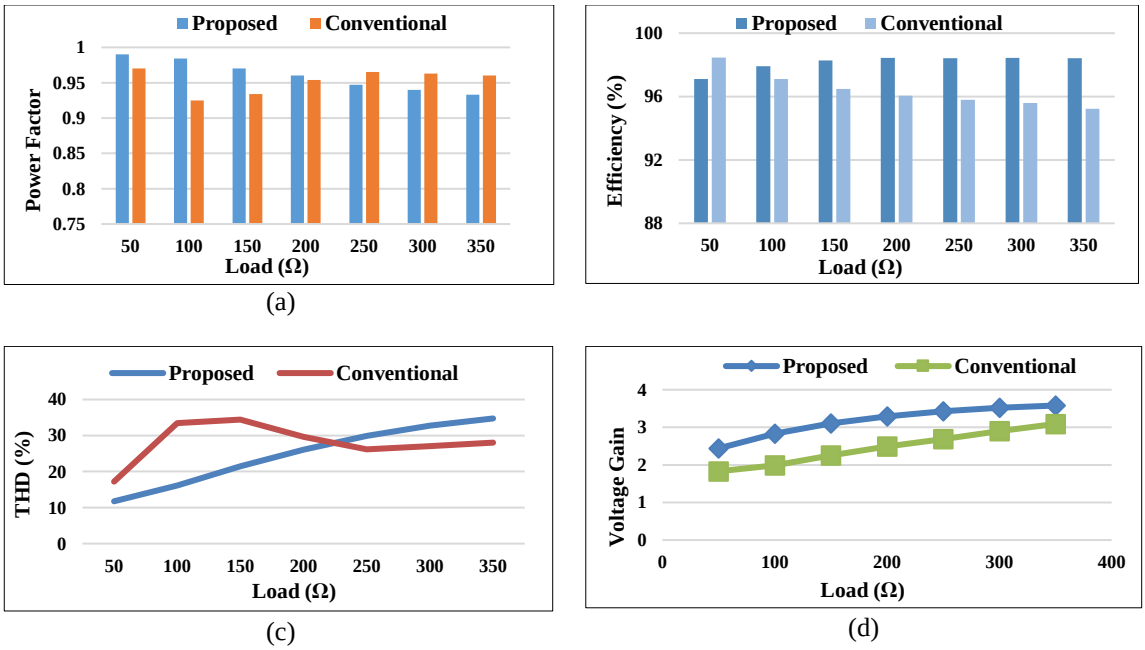

Figure 7. Graphic contrast of; (a) input PF, (b) efficiency (%), (c) THD (%), and (d) voltage gain amid proposed and conventional converter with load variation

4.3. Performance study under switching frequency (Fs) variation

The proposed and conventional converters both are simulated with the same load of 100 Ω and the same duty ratio of 0.5. The performance of both converters is analyzed under switching frequency variation (10 KHz to 100 KHz). From Figure 8(a) we can see that the input PF is higher in the case of the proposed converter compared to the conventional converter over frequency variation. The difference in PF is clearly visible as the lowest PF of the proposed converter is 0.979 whereas the conventional converter can achieve a maximum PF of 0.925. In terms of conversion efficiency, the conventional converter shows better performance over the change of frequency except for the frequency of 10 k where the suggested circuit has greater efficiency as observed in Figure 8(b). The suggested converter provides superior results in consideration of input current THD compared to the conventional one throughout frequency variation as observed in Figure 8(c). The proposed converter can maintain THD below 20% for almost all the frequencies whereas the lowest THD achieved by conventional converter is 33.43%. As noticed from Figure 8(d), the suggested topology caters a higher boost voltage than the conventional one over the change of frequency. The voltage boosting exceeds 3 times for the proposed converter where the maximum boosting the conventional converter provides is 1.9 times.

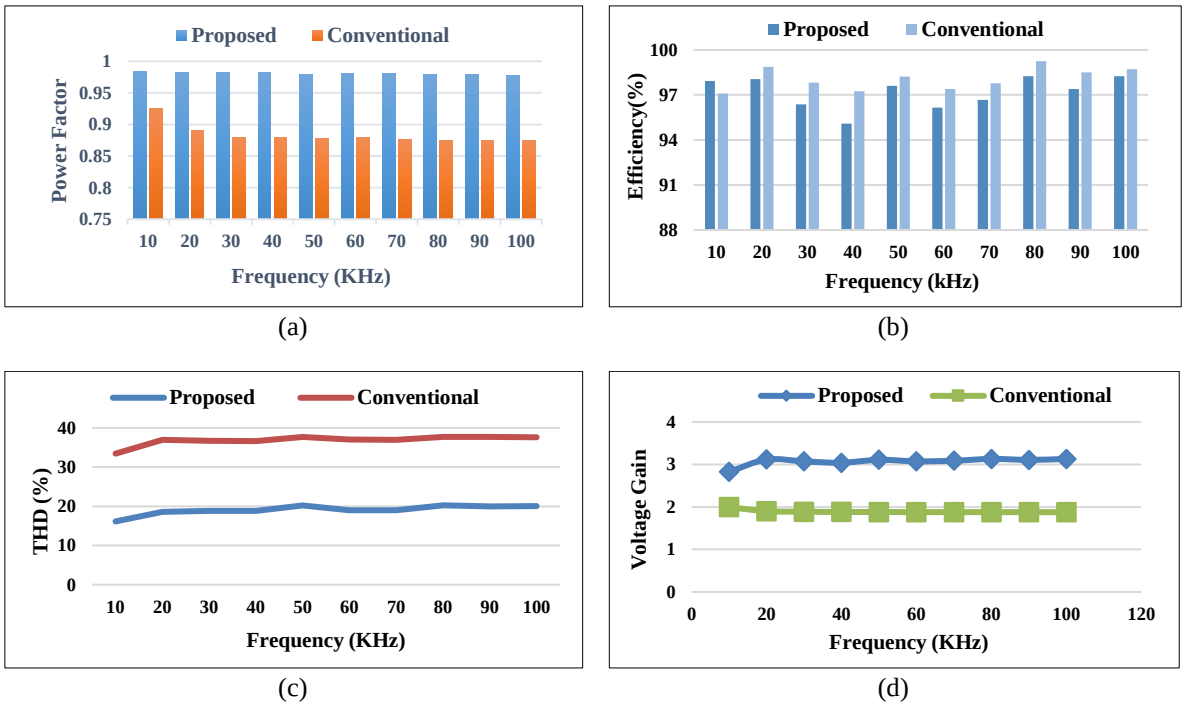

Figure 8. Graphical comparison of; (a) input PF, (b) efficiency (%), (c) THD (%), and (d) voltage gain of the proposed QBC with conventional boost over frequency variation

5. PROPOSED QBC WITH FEEDBACK AND CONTROL

The feedback controller is designed for the suggested converter for improvement of the PF and keep THD below 10% (considering the fundamental frequency component) as per the standard of IEC 61000-3-2 and IEC 61000-3-4 [23]. In general, PFC control is comprised of two loops, one is inner loop and other is outer loop. The inductor current is controlled by the inner loop whereas the outer loop maintains the average DC output voltage. A dual-loop feedback controller is used for the proposed converter as seen in Figure 9.

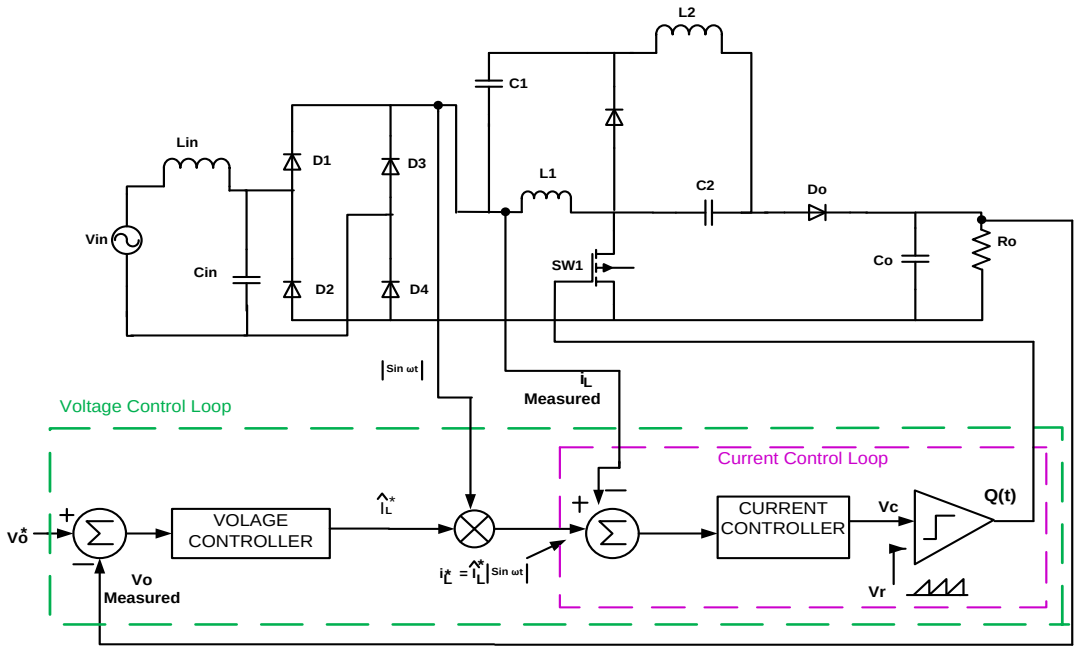

Figure 9. Dual loop feedback controller for the proposed converter

Here, i_L^* represents the inductor current (reference) which is in rectified form (full wave). Two control loops are directed based on the prerequisites of the form and the inductor current's magnitude for performing pulse-width modulation on the switch of the proposed QBC. The current control loop is depicted within the inner dotted box on the right side of Figure 7. The loop uses an average-current-mode control to pursue the reference with the least possible THD. In this control scheme the error amidst the i_L^*(t) and i_L(t) is amplified by the current controller to avail the control voltage, V_c(t). V_c(t) is then used in comparison between itself and a ramp signal V_r(t) in the PWM controller IC to generate the switching sequence, Q(t). The output voltage is taken as feedback and using this signal the exterior voltage control loop regulates $\hat{I}_L$, the magnitude of i_L^*. Voltage feedback helps the outer loop adjust $\hat{I}_L$ to retrieve the O/P voltage to its reference value.

6. SIMULATION RESULTS WITH FEEDBACK CONTROLLER

Simulation is carried out for the suggested converter with a feedback controller. The controller is constructed to attain an average of 1000 V DC at output side for a load of 100 Ω. From Figure 10, we can see that supply voltage and supply current are almost in phase which results in nearly unity PF.

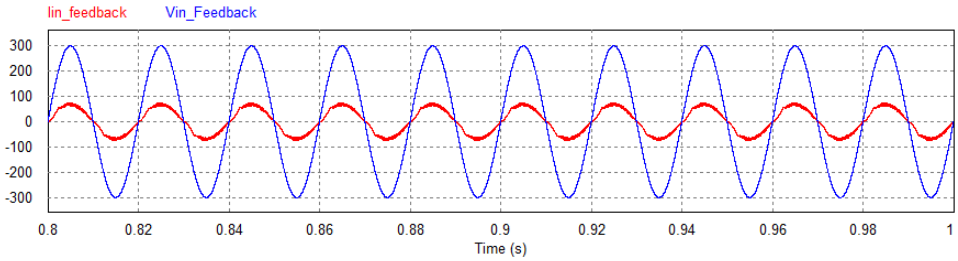

Figure 10. Wave shape of input voltage (Vin) and input side current (Iin) of the suggested converter with feedback controller

Figure 11 shows that there is negligible higher order harmonics in the frequency spectrum of the input side current. The simulated results are given in Table 2. It is evident that the proposed QBC with closed loop controller has superior input PF than conventional and QBC without feedback controller. Current THD in input side is 7.45% for feedback controlled QBC which is notably better than conventional and QBC without feedback.

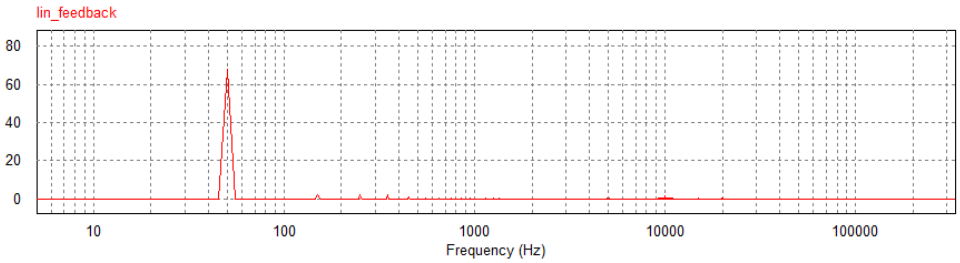

Figure 11. The frequency spectrum of Iin of the suggested converter with feedback control

Table 2. Comparison of simulated results

Performance parameters	Conventional boost	Proposed quadratic boost without feedback	Proposed quadratic boost with feedback
Input PF	0.93	0.97	0.997
Input current THD	33.70%	14.30%	7.45%

7. CONCLUSION

A novel AC-DC QBC has been designed and reported with different performance analysis. A thorough investigation is performed of the proposed converter's PF, conversion efficiency, input current THD, and voltage gain varying duty cycles, output load, and switching frequency and contrasted with the traditional boost converter. The theoretical output voltage and simulated output voltage are in close

concession with one other which determines the efficacy of this design. The efficiency, PF, THD and voltage gain of the designed converter at a D value of 50% are 97.92%, 0.98, 16.14, and 2.83 respectively at a fixed output load of 100 Ω. The notable advantage of the suggested converter is that it provides highly regulated output voltage with a PF values up to 0.99 and moderate THD of 7.45% when a dual loop voltage and current controller is used. It is observed that the proposed converter provides near unity PF and low THD for various output load, and D values. The suggested converter is deemed to be convenient to employ for an extensive range of load and switching frequencies based on the results described in this paper which make it ideal for appliances where high O/P voltage gain is needed at low input THD and high PF without using any additional power switches or transformer based isolated magnetic components.

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