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Modified multicarrier sinusoidal pulse-width modulation for three-phase open-load five-level inverter

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ABSTRACT

Five-level voltage source inverter (VSI) is a power inverter topology generating a five-level output voltage waveform. This inverter topology can reduce harmonics distortion to be lower compared to a conventional two-level inverter. In practical, delay of gating signals is unavoidable during switching operation of power semiconductor switches. Adding dead time in the gating signals of VSI's power switches is mandatory to avoid short circuit during switching operation. However, the dead time of the inverter's switching signals causes low frequency harmonics and distortion of inverter's output waveforms. In this paper, a different multicarrier sinusoidal pulse-width modulation (SPWM) method with harmonics suppression capability was proposed and applied in the three-phase open-connection load five-level inverter. The proposed modified SPWM was tested using computer simulation of Powersim (PSIM) software. The measured output waveforms of the five-level VSI at different power factor conditions are presented and analyzed. The total harmonics distortion (THD) values of inverter's output current were suppressed using the proposed SPWM method to be less than 1%. The test results showed that the proposed modified SPWM method was able to reduce the distortion (THD) of alternating current (AC) waveform, and increase the quality of the inverter's output power.

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1. INTRODUCTION

Power inverter is a power electronic converter having capability to convert direct current (DC) power into alternating current (AC) power with controllable frequency, phase angle, and magnitudes of its output voltage and current waveforms. Currently, power electronic inverters play a crucial role in modern electrical systems, enabling the efficient and flexible conversion of DC power to AC power for a wide range of applications such as industrial processes, electric vehicles, consumer electronics, household equipments, power system controllers, and renewable energy systems for example in photovoltaic (PV) and wind power generations. The power inverter plays a central role in AC motor drive applications, enabling precise control over the operation of AC motors [1], [2]. In grid-tied PV systems, power inverters convert the DC electricity generated by solar panels into AC electricity that can be used in buildings or fed back into the grid [3]–[5]. In wind energy systems, inverters are used to convert the variable-speed AC output of wind turbines into stable AC electricity suitable for AC power load or grid connected operation [6], [7].

A two-level inverter is one of the simplest types of inverters used in power electronics. It's called "two-level" because it has two voltage levels: a positive and a negative voltage level [8], [9]. This inverter is

widely used in various applications due to their simplicity and cost-effectiveness, although they may have some drawbacks such as higher harmonic content. Moreover, this inverter generates large gradient voltage of its output waveform [10]–[12]. In scenarios where low harmonic distortion or higher voltage levels are required, more advanced inverter topologies may be preferred. Improvement of power inverter performance has become a challenge for researchers in power electronics area.

Development of new topologies of power inverter is a strategy to obtain power inverter with better performance such as increasing power quality, power capacity, efficiency, and power density of inverter circuits. Multilevel inverter topology is an alternative solution of these issues. A multilevel inverter is a type of power electronic inverter that generates an AC output waveform by synthesizing multiple voltage levels from several or single DC sources. Unlike traditional two-level inverters, which have only two voltage levels (positive and negative), multilevel inverters can produce several discrete voltage levels, resulting in a smoother output waveform with reduced harmonic distortion [13]–[16]. Moreover, lower electromagnetic interference (EMI) and lower dv/dt stress on motor windings in motor drive applications can be achieved using this inverter [17]–[21].

On the other hand, development of new control techniques and methods for better operation of inverters is another alternative solution to improve the inverter performance. Sinusoidal pulse-width modulation (SPWM) is a method of pulse width modulation applied in inverters to generate a sine wave from a DC input. SPWM works comparing a sinusoidal reference signal with a triangular carrier wave and producing gating pulses that vary in width according to the amplitude of the sine wave. SPWM is a practical and widely used pulse-width modulation (PWM) method for digital controlled voltage-source type converters [22]–[24]. In the multilevel inverter application, multi carriers SPWM is a technique to generate lower distortion of AC output waveform. Instead of a single triangular carrier signal used in SPWM, multi carrier SPWM employs multiple carrier signals. These carrier signals are typically triangular waves with frequencies that are integer multiples of the fundamental frequency of the reference signal. By using multiple carrier signals, it can distribute the harmonic content across a wider frequency spectrum compared to single-carrier techniques like SPWM. This helps in reducing harmonic distortion in the output waveform [25]–[27].

In practical manner, dead-time was required and applied in the gating signals of inverter power switches especially in the voltage source inverter (VSI) type. Dead time in an inverter refers to a brief interval during which both the high-side and low-side switches of the inverter are turned off simultaneously to prevent shoot-through current, which can damage the switches and cause inefficiencies in the system. Shoot-through current occurs when both switches are conducting simultaneously, creating a short circuit across the DC source. However, the dead time introduces a small delay in the switching transitions, which can affect the performance of the inverter, especially at high frequencies. The dead time introduced distortion in the output waveform and affect the overall performance of the inverter [28]–[30]. Therefore, dead time compensation techniques may be employed to minimize the impact of dead time on system performance. Dead time compensation techniques are essential in high-performance inverter systems where precise control of the output waveform is required, such as ac motor drives, renewable energy systems, and grid-connected inverters. By minimizing the effects of dead time, it will help to improve power quality, reduce distortion, and enhance the overall performance of the power electronics inverter system [31], [32]. A method to compensate the effect of deadtime in a single phase H-bridge VSI has been proposed and discussed in [33]. However, the inverter circuit is a single phase three-level VSI type.

In this paper, a modified multicarrier SPWM technique is proposed to minimize the distortion of inverter's AC output wave caused by dead time effect. The proposed method was applied in a five-level VSI with open-end connection loads previously developed by Suroso *et al.* [34] to improve its performance. The proposed SPWM and five-level inverter were tested through computer simulation with PSIM software at several different conditions, i.e., load power factor, modulation index, and dead time values. Moreover, the test results were analyzed and compared with the conventional SPWM to validate the effectiveness of the proposed SPWM technique.

2. POWER INVERTER CIRCUITS AND PROPOSED MODULATION METHOD

Figure 1 presents the circuits of three phase five-level inverter with open-end connection load. It consists of nine teen insulated gate bipolar transistors (IGBTs) in total to build the inverter circuits. This inverter works converting a single DC power source into three phase output voltage for open-end connection loads. Figure 2 shows the conventional SPWM method. This SPWM method utilized four triangular carrier signals, V_{cr1}, V_{cr2}, V_{cr3}, and V_{cr4}. These triangular carrier waves have identic frequency, the same phase angle and peak-to-peak magnitude. The frequency of these carrier signals controls the switching frequency of IGBT switches employed in the inverter. The signals V_r, V_s, and V_t are the enlarged sinusoidal modulating waveforms which are three sinusoidal signals with 120° phase difference. Frequency of modulating signals determine the main frequency of the inverter's output current wave.

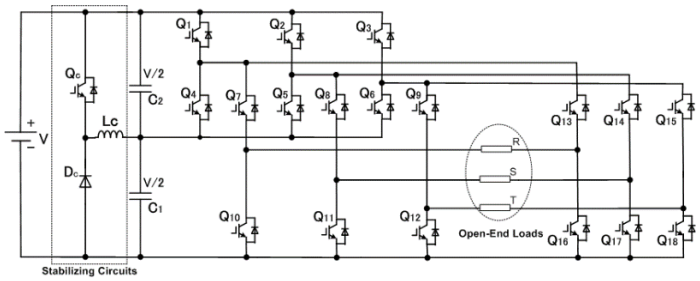

Figure 1. Five-level power inverter system [34]

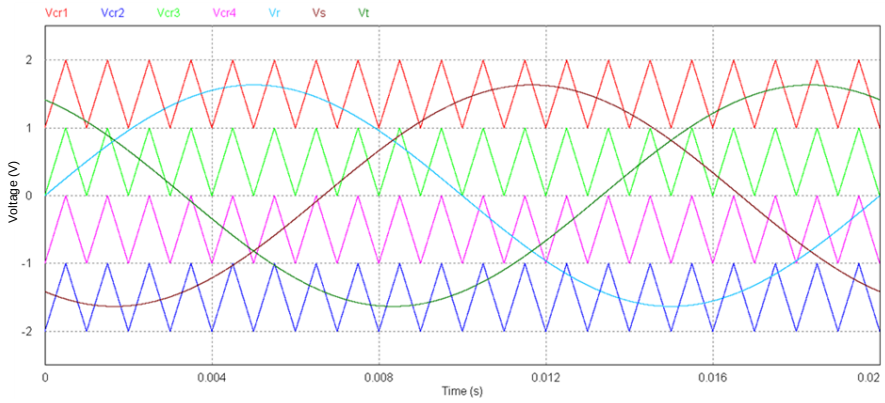

Figure 2. Conventional SPWM technique [34]

Moreover, Figure 3 is the proposed modified level shifted multi carrier signals SPWM. It requires four carrier signals, i.e., $V_{cr1'}$, $V_{cr2'}$, $V_{cr3'}$, and $V_{cr4'}$ as depicted in Figure 3(a). An obvious distinction compared to the traditional SPWM is the crossing between the lower and upper carrier waves. This intersected area is not existed in the conventional SPWM technique of Figure 2. The more detail figure of this SPWM technique is shown in Figure 3(b). In Figure 3(b), the driving signal of IGBT switch with modified SPWM is the G*. It is produced by the proposed SPWM technique. The value of dead-time is ΔT. This figure depicts the feature of the SPWM strategy where the loss voltage pulse produced by the dead-time is minimized. The loss voltage signal indemnified by the proposed SPWM method is indicated as ΔV_o*. The voltage pulse losses ΔV_o cerated by the dead-time will be minimized.

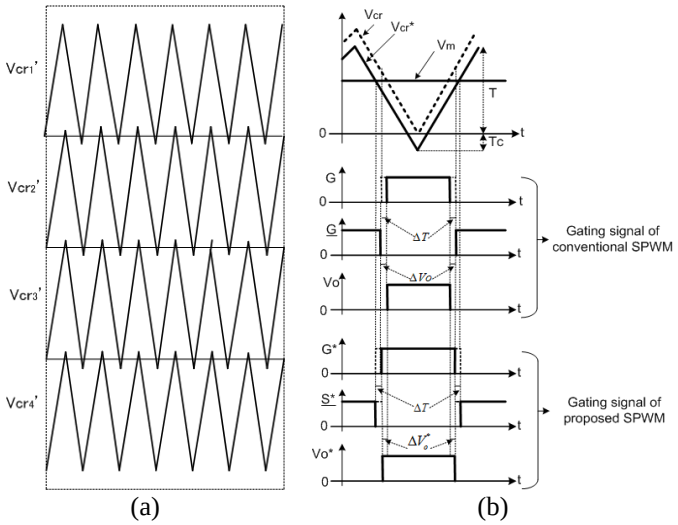

Figure 3. Proposed modified level shifted multi carrier signals SPWM; (a) proposed modified SPWM technique and (b) enlarged figure of modifed SPWM technique

If the crossing parts between two carrier signals V_{cr1}' and V_{cr2}' is σ, which is named as the percentage of cross area. The percentage value of σ can be calculated as (1):

$$o = \frac{(V_{cr1}' - AV_{cr2}')}{V_{cr2}'} \times 100\% \quad (1)$$

waveform distortion of an AC waveform containing harmonics components can be calculated using formula of total harmonics distortion (THD) as (2):

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + \cdots + I_n^2}}{I_1} \times 100\% \quad (2)$$

where I_2, I_3, and I_n are the second, third and n^{th} harmonics orders, I_1 is the fundamental component of AC waveform.

3. RESULTS AND DISCUSSION

The proposed modified SPWM technique was tested for three-phase five-level inverter of Figure 1 using computer simulation of PSIM software with test parameters shown in Table 1. The main input DC voltage was 100 V. So, the input capacitors voltage of inverter will be set as 50 V. The switching frequency of IGBT switches was 20 kHz in order to push the harmonics components of inverter's output current into high frequency band. The main frequency of output voltage was 50 Hz, which was the grid frequency of domestic electric utility. To filter the harmonics components of inverter's output waveform, power inductors 0.01 mH and capacitors 50 μF were implemented as power filter. The inverter circuit was connected to a three-phase open-end inductive resistor power load, i.e., resistor 20 Ω and inductor 5 mH for each phase.

Table 1. Circuit parameters

Parameters	Value
Input voltage	100 V
Switching frequency	20 kHz
Output frequency	50 Hz
Output filter	L=0.01 mH, C=50 μF
Power load	R=20 Ω, L=5 mH

Figure 4 shows the output waveforms of current and load voltage of inverter circuits. Three-phase sinusoidal current waveforms, i.e., I_r, I_s, and I_t were generated by inverter. Moreover, three-phase five-level pulse-width modulation (PWM) voltage waveforms V_r, V_s, and V_t were confirmed in this inverter circuit. The THD profile of load current for different modulation indexes of PWM method is presented in Figure 5. This test result is for ideal condition where dead-time was not added in the gating signals of IGBT power switches. The lowest THD value of 0.897 was achieved at modulation index around 1.

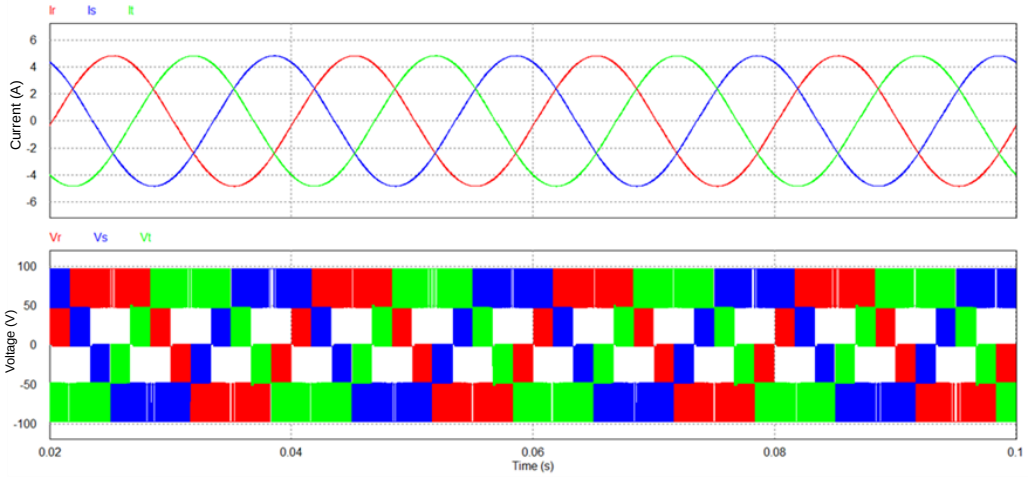

Figure 4. Output current and voltage waveforms of inverter circuits

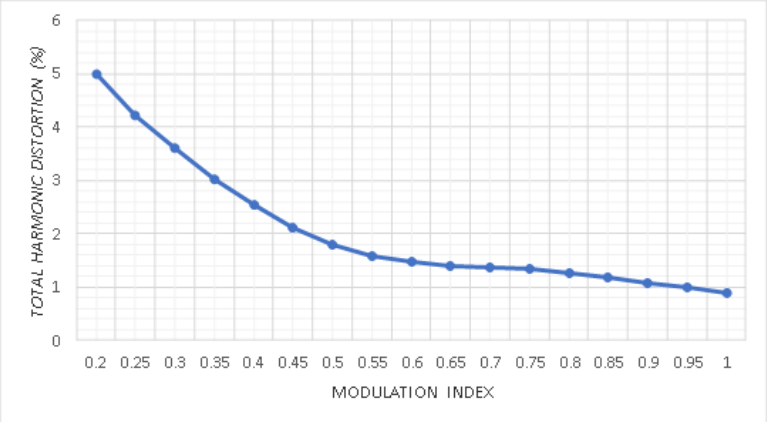

Figure 5. THD characteristic of inverter's output current without dead-time

Test results of THD profile of inverter's switches gating signals with dead-time is shown in Figure 6. The dead-time value in this test was varied as 4 µs and 6 µs. As can be observed in the figure, the THD value at dead-time 6 µs was higher than at dead-time 4 µs. These tests were conducted for conventional SPWM method as previously depicted in Figure 2. Figure 7 is the THD profile comparison for conventional and proposed modified SPWM method of inverter output current for dead-time delay 4 µs at load power factor 0.5. As shown in this figure, the THD value of inverter's output current was suppressed using the proposed SPWM method to be less than 1%.

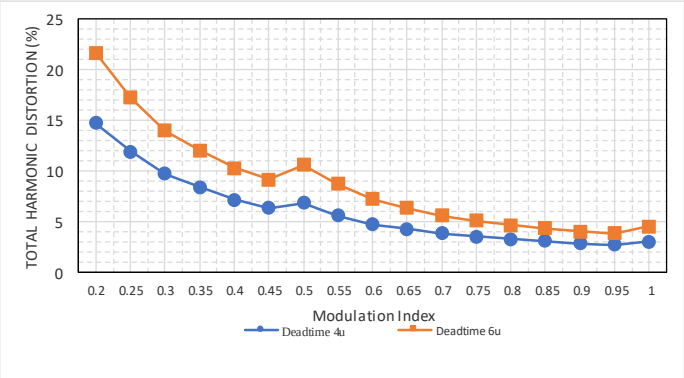

Figure 6. THD characteristic of inverter output current with dead-time 4 µs and 6 µs

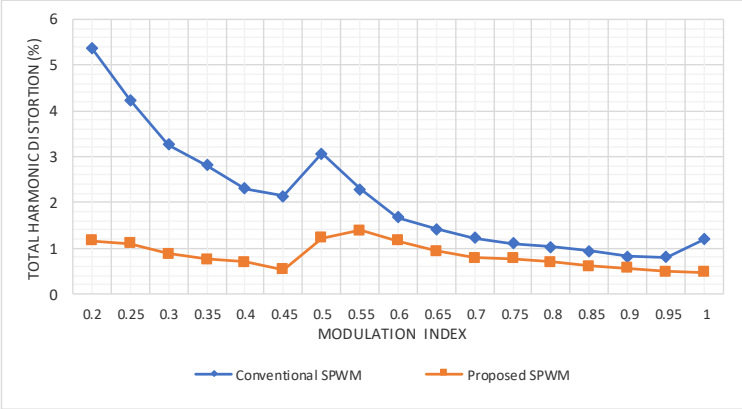

Figure 7. THD profile of inverter's output current for conventional and proposed SPWM with dead-time 4 µs at phase fraction (PF)=0.5

A comparison of low harmonics components, i.e., 3rd, 5th, 7th, 9th, 11th, and 13th orders for conventional and proposed SPWM methods is shown in Figure 8. The magnitude of the 3rd and 7th harmonics decreased from 0.6% into 0.23%, and 0.21% into 0.04, respectively. Moreover, the test results at power factor 0.9 are presented in Figures 9 and 10. In this case, the magnitude of low harmonics was also reduced. Figure 11 presents characteristic of THD versus cross area value of triangular carrier waves for different deadtime values. In case of dead time 4 µs, the minimum value of THD was achieved at cross area value (σ) around 10%. When the dead time value was 3 µs, the optimum THD value was achieved at crossing area value of σ at 7%. A lower deadtime value needs a lower crossing area value between triangular carriers. However, smaller deadtime value needs better performance of power semiconductor swithes. The proposed SPWM method was confirmed capable in reducing THD values and the magnitudes of low harmonics component of inverter's AC output current caused by dead time.

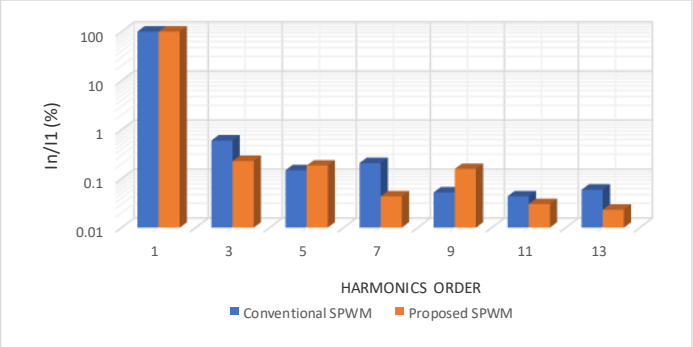

Figure 8. Low order harmonics comparison of output current for conventional and proposed SPWM with dead-time 4 µs at PF=0.5

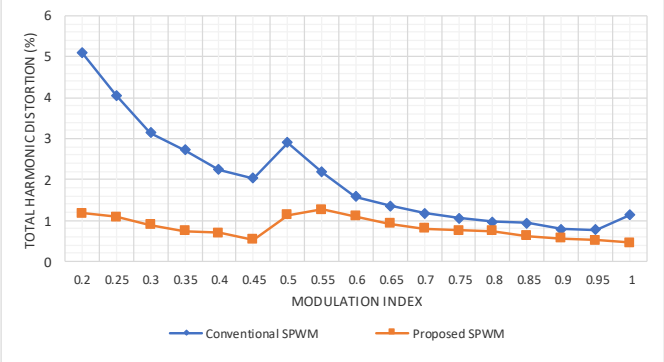

Figure 9. THD profile of inverter's output current for conventional and proposed SPWM with dead-time 4 µs at PF=0.9

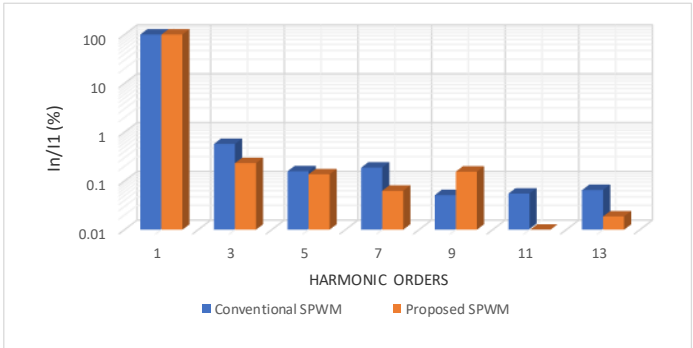

Figure 10. Low order harmonics comparison of inverter's output current for conventional and proposed SPWM with dead-time 4 µs at PF 0.9

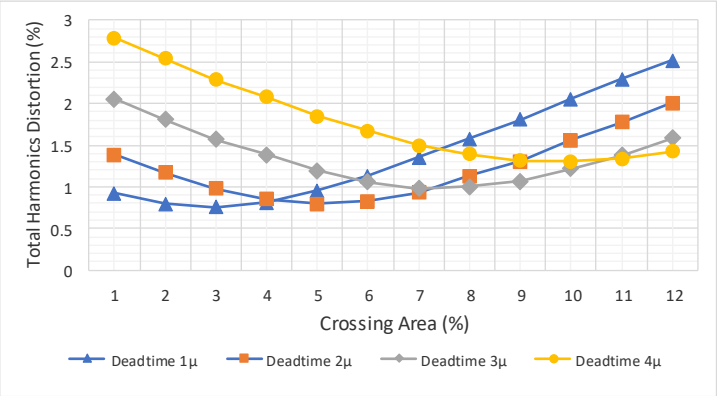

Figure 11. Characteristic of THD versus cross area of triangular carrier waves for different deadtime values

4. CONCLUSION

A modified multicarrier SPWM method was proposed and discussed in the paper. The proposed modified SPWM introduced a feature in reducing harmonics component and distortion of inverter's output current waveform caused by dead time of inverter circuits. The modified SPWM was implemented and tested for a three-phase five-level inverter. The power inverter circuits supplied a three-phase independent load. The test results showed that the proposed SPWM method was capable in reducing the magnitudes of low harmonics components and waveform distortion (THD) values of inverter's output current. In case of inductive-resistive load, if the load power factor closer to be 1, the resulting THD value will be smaller, while the output current will become a better sinusoidal waveform.

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REFERENCES

[1] B. Kwak, J. H. Um, and J. K. Seok, "Direct active and reactive power control of three-phase inverter for AC Motor drives with small DC-link capacitors fed by single-phase diode rectifier," *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 3842–3850, Jul. 2019, doi: 10.1109/TIA.2019.2915061.

[2] M. Tousizadeh, H. S. Che, J. Selvaraj, N. A. Rahim, and B. T. Ooi, "Performance comparison of fault-tolerant three-phase induction motor drives considering current and voltage limits," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2639–2648, Apr. 2019, doi: 10.1109/TIE.2018.2850006.

[3] J. M. Carrasco *et al.*, "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006, doi: 10.1109/TIE.2006.878356.

[4] I. G. C. Raj, M. Kaliamoorthy, V. Rajasekaran, and R. M. Sekar, "Single-phase cascaded grid connected multilevel inverter for interfacing renewable energy sources with microgrid," *Journal of Solar Energy Engineering*, vol. 137, no. 5, Oct. 2015, doi: 10.1115/1.4030886.

[5] Suroso and H. Siswantoro, "A performance comparison of transformer-less grid tied PV system using diode clamped and neutral point shorted inverters," *International Journal of Power Electronics and Drive Systems*, vol. 11, no. 2, pp. 702–710, Jun. 2020, doi: 10.11591/ijpeds.v11.i2.pp702-710.

[6] K. Arthishri, N. Kumaresan, and N. A. Gounden, "Analysis and application of three-phase SEIG with power converters for supplying single-phase grid from wind energy," *IEEE Systems Journal*, vol. 13, no. 2, pp. 1813–1822, Jun. 2019, doi: 10.1109/JSYST.2018.2875761.

[7] C. Yuan, X. Zhou, and Y. Ma, "DC bus voltage control of wind power inverter based on first-order LADRC," *IEEE Access*, vol. 10, pp. 3263–3274, 2022, doi: 10.1109/ACCESS.2021.3138274.

[8] T. Qanbari and B. Tousi, "Single-source three-phase multilevel inverter assembled by three-phase two-level inverter and two single-phase cascaded H-bridge inverters," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5204–5212, May 2021, doi: 10.1109/TPEL.2020.3029870.

[9] Z. H. Bai and Z. C. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2260–2267, Sep. 2008, doi: 10.1109/TPEL.2008.2001893.

[10] S. Suroso, A. N. Aziz, and T. Noguchi, "Five-level PWM Inverter with a single DC power source for DC-AC power conversion," *International Journal of Power Electronics and Drive Systems*, vol. 8, no. 3, p. 1212, Sep. 2017, doi: 10.11591/ijpeds.v8.i3.pp1212-1219.

[11] Y. Zuo, X. Zhu, X. Si, and C. H. T. Lee, "Fault-tolerant control for multiple open-leg faults in open-end winding permanent magnet synchronous motor system based on winding reconnection," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 6068–6078, May 2021, doi: 10.1109/TPEL.2020.3030237.

[12] R. J. Kerkman, D. Leggate, D. W. Schlegel, and C. Winterhalter, "Effects of parasitics on the control of voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 140–150, Jan. 2003, doi: 10.1109/TPEL.2002.807190.

[13] D. Ruiz-Caballero, R. Sanhueza, H. Vergara, M. Lopez, M. L. Heldwein, and S. A. Mussa, "Cascaded symmetrical hybrid multilevel Dc-Ac converter," in *2010 IEEE Energy Conversion Congress and Exposition*, Sep. 2010, pp. 4012–4019, doi: 10.1109/ECCE.2010.5617805.
[14] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 51–65, Jan. 2011, doi: 10.1109/TPEL.2009.2031115.
[15] Suroso, A. Mubyarto, and T. Noguchi, "A different single-phase hybrid five-level voltage- source inverter using DC-voltage modules," *Telecommunication Computing Electronics and Control*, vol. 12, no. 3, pp. 557–562, Sep. 2014, doi: 10.12928/v12i3.78.
[16] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 922–929, Feb. 2015, doi: 10.1109/TIE.2014.2336601.
[17] Y. Tadano, S. Urushibata, K. Ogura, A. Shigaki, and M. Nomura, "A multilevel PWM strategy suitable for high-voltage motor direct drive systems in consideration of the adverse effect of a deadtime," *IEEJ Transactions on Industry Applications*, vol. 126, no. 1, pp. 1–9, 2006, doi: 10.1541/ieejias.126.1.
[18] B. P. Reddy and S. Keerthipati, "A multilevel inverter configuration for an open-end-winding pole-phase-modulated-multiphase induction motor drive using dual inverter principle," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3035–3044, Apr. 2018, doi: 10.1109/TIE.2017.2750626.
[19] V. T. Somasekhar, S. Srinivas, B. P. Reddy, C. N. Reddy, and K. Sivakumar, "Pulse width-modulated switching strategy for the dynamic balancing of zero-sequence current for a dual-inverter fed open-end winding induction motor drive," *IET Electric Power Applications*, vol. 1, no. 4, pp. 591–600, 2007, doi: 10.1049/iet-epa:20060407.
[20] S. Jain, A. K. Thopukara, R. Karampuri, and V. T. Somasekhar, "A single-stage photovoltaic system for a dual-inverter-fed open-end winding induction motor drive for pumping applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4809–4818, Sep. 2015, doi: 10.1109/TPEL.2014.2365516.
[21] W. Hu, C. Ruan, H. Nian, and D. Sun, "Simplified modulation scheme for open-end winding PMSM system with common DC bus under open-phase fault based on circulating current suppression," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 10–14, Jan. 2020, doi: 10.1109/TPEL.2019.2924821.
[22] R. Sarker, A. Datta, and S. Debnath, "FPGA-based high-definition SPWM generation with harmonic mitigation property for voltage source inverter applications," *IEEE Transactions on Industrial Informatics*, vol. 17, no. 2, pp. 1352–1362, Feb. 2021, doi: 10.1109/TII.2020.2983844.
[23] Z. Liu, Z. Zheng, S. D. Sudhoff, C. Gu, and Y. Li, "Reduction of common-mode voltage in multiphase two-level inverters using SPWM with phase-shifted carriers," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6631–6645, Sep. 2016, doi: 10.1109/TPEL.2015.2499380.
[24] J. Huang and R. Xiong, "Study on modulating carrier frequency twice in SPWM single-phase inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3384–3392, Jul. 2014, doi: 10.1109/TPEL.2013.2280395.
[25] J. Lyu, W. Hu, F. Wu, K. Yao, and J. Wu, "Variable modulation offset SPWM control to balance the neutral-point voltage for three-level inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7181–7192, Dec. 2015, doi: 10.1109/TPEL.2015.2392106.
[26] M. Narimani, B. Wu, and N. R. Zargari, "A novel five-level voltage source inverter with sinusoidal pulse width modulator for medium-voltage applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1959–1967, Mar. 2016, doi: 10.1109/TPEL.2015.2440656.
[27] D. Karthikeyan, R. Palanisamy, K. Vijayakumar, A. Velu, and D. Selvabharathi, "Parallel connected VSI inverter using multi-carrier based sinusoidal PWM technique," *Telecommunication Computing Electronics and Control*, vol. 15, no. 4, pp. 1625–1631, Dec. 2017, doi: 10.12928/TELKOMNIKA.v15i4.6477.
[28] S. Ahmed, Z. Shen, P. Mattavelli, D. Boroyevich, and K. J. Karimi, "Small-signal model of voltage source inverter (VSI) and voltage source converter (VSC) considering the deadtime effect and space vector modulation types," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4145–4156, Jun. 2017, doi: 10.1109/TPEL.2016.2595568.
[29] A. Guha and G. Narayanan, "Small-signal stability analysis of an open-loop induction motor drive including the effect of inverter deadtime," *IEEE Transactions on Industry Applications*, vol. 52, no. 1, pp. 242–253, Jan. 2016, doi: 10.1109/TIA.2015.2464305.
[30] H. S. Kim, Y. C. Kwon, S. J. Chee, and S. K. Sul, "Analysis and compensation of inverter nonlinearity for three-level t-type inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4970–4980, Jun. 2017, doi: 10.1109/TPEL.2016.2607226.
[31] C. D. Townsend, G. Mirzaeva, and G. C. Goodwin, "Deadtime compensation for model predictive control of power inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7325–7337, Sep. 2017, doi: 10.1109/TPEL.2016.2630712.
[32] D. H. Lee and J. W. Ahn, "A simple and direct dead-time effect compensation scheme in PWM-VSI," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3017–3025, Sep. 2014, doi: 10.1109/TIA.2014.2303932.
[33] Suroso, D. T. Nugroho, and T. Noguchi, "New dead-time compensation method of power inverter using carrier based sinusoidal pulse-width modulation," *International Journal of Electrical and Computer Engineering*, vol. 8, no. 6, pp. 4880–4891, 2018, doi: 10.11591/ijece.v8i6.pp4880-4891.
[34] Suroso, D. T. Nugroho, and T. Noguchi, "A different voltage-source power inverter with carrier based SPWM for open-end connection loads," *Energies*, vol. 12, no. 17, p. 3251, Aug. 2019, doi: 10.3390/en12173251.

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