Bulletin of Electrical Engineering and Informatics
Vol. 13, No. 6, December 2024, pp. 3993~4001
ISSN: 2302-9285, DOI: 10.11591/eei.v13i6.8594

Exploring the synergy: AI and ML in very large scale integration design and manufacturing

Sima K. Gonsai[1], Kinjal Ravi Sheth[1], Dhavalkumar N. Patel[1], Hardik B. Tank[1], Hitesh L. Desai[1], Shilpa K. Rana[2], Suresh Laxmanbhai Bharvad[1]
[1]Department of Electronics and Communication, L. D. College of Engineering, Ahmedabad, India
[2]Department of Electronics and Communication, Government Engineering College, Modasa, India

Article Info

Article history:

Received Apr 16, 2024
Revised Jun 28, 2024
Accepted Aug 7, 2024

Keywords:

Deep learning
Fault coverage
Integrated circuit testing
Machine learning
Very large scale integration chip design

ABSTRACT

With the rapid advancements in very large scale integration (VLSI) and integrated circuit (IC) technology, the complexity of devices has escalated significantly. Designing a VLSI chip is essential for scaling up the capabilities of chips to meet the growing demands of modern applications, like artificial intelligence (AI), IoT, and high-performance computing. Chip testing and verification also emerges as crucial tasks to ensure optimal device functionality. Testing verifies the integrity of a circuit's gates and connections, ensuring accurate operation. Throughout the chip's design and development life cycle, design, testing and verification composes a substantial portion of the effort. AI and machine learning (ML) are used in many different research domains to improve predicted accuracy, automate difficult jobs, provide data-driven insights, and optimise workflows. This study aims to showcase the vital role of AI/ML in reducing complexity in VLSI chip design life cycle by automating test pattern generation and fault detection, enhancing efficiency and accuracy, and significantly reducing the time and resources needed for design verification and optimization.

Corresponding Author:

Kinjal Ravi Sheth
Department of Electronics and Communication, L. D. College of Engineering
Ahmedabad, Gujarat-380015, India
Email: krsheth@ldce.ac.in

1. INTRODUCTION

The introduction of complementary metal-oxide semiconductor (CMOS) transistors in the integrated circuit (IC) sector has sparked a significant change in the field of electronics, in the field of semiconductor devices [1]. As CMOS technology has dominated the microelectronics industry, since the 1960s, the number of transistors produced on a single chip has grown tremendously. The density of the devices has exponentially grown due to drastically reduction in transistor dimensions [2]. It leads to huge growth in very large scale integration (VLSI) industry. Demand for energy efficient, faster, compact and cost effective designs with advance features has substantially expanded in recent years due to the rising demand for portable gadgets for online education, gaming, video on demand, and online business. Research in IC technology has brought the scale to as low as 2 nm technology [3].

Very fast and rapid growth of VLSI industry has brought both opportunities and challenges in chip design and manufacturing. Verification, testing and entire stages of SoCs complexity increased a lot during chip design. As the device dimension decreases, certain performance parameters tend to degrade, leakage current tends to increase [4], [5], gain reduces and process changes variations increments [6]. The design functioning is greatly affected by the rise in process variations, which results in inconsistent performance in transistors of the same dimension. It also affects the circuit's propagation delay, which behaves like a random variable and makes timing-closure approaches more challenging and has a significant impact on chip yield [7]. However, Yield loss degrades due to high reduction in dimensionality of transistor in nanometer regime. Compared to CMOS, multi-gate field-effect transistors (FETs) [8] are more prone to processing variations. High scaling also has an impact on their performance metrics [9], [10]. To simulate circuits for structural testing, and delay measurements, a number of electronic design automation (EDA) tools for fault identification and test pattern generation are available, where advanced optimization technique is adopted in the entire VLSI design cycle [11]. The effectiveness of EDA tools in overcoming design issues determines time to quickly produce a chip. A traditional design method in EDA tools takes large time to provide faster and optimal solution of the design constraints. Moreover, some NP-complete problems, which are prevalent in the chip design and computer-aided design (CAD) sector, can be solved using machine learning (ML) techniques, whereas conventional approaches are time consuming need significant resources. So, time to market for the chip manufacturing largely depends on efficacy of the EDA tools and its methodology in implementation of the design process.

Artificial intelligence-ML (AI-ML) has provided significant solutions to the very well-known real-life problems. The existence of graphics processing unit (GPU) based convolutional and deep neural networks (DNNs) are enabling researchers in almost every discipline, including green field work, communications, medicine, and all branches of engineering, to explore using ML for addressing highly complex and difficult problems. ML has seen as a revival in recent years, with applications in fields as diverse as automating discovery of the drug and predicting failure of the turbine of wind [12]. The basic idea is to mimic the behavior and intelligence of human specifically 'human brain' in providing solutions using machines of different complexities. ML is sub category of AI. AI-ML is basically learning from the dataset and determine the relation between input and output, to predict the result of unseen data. It quickly interprets the results based on inputs available in the large dataset and enables humans to make faster and correct solutions of the problem. ML can operate large datasets at high speed with the help of high-end processing units like GPUs. With each incremental addition of data in the set, machine further adds experience and improves on the efficiency of the predictions. It also helps in decision making of the crucial points in process and design cycle. Applicability of AI/ML penetrates in all the fields of research and technology. Since 2010, ML algorithms have held their place and entered the VLSI design and development domain.

At every stage of VLSI design flow, different CAD tools are involved, from specifications to Tap out, final chip manufacturing. Digital, analog and mixed signal IC's performance quality largely depends on the capabilities of these CAD tools. With tremendously high increase of transistors per unit chip area demand advancement in CAD tools, which is even more challenging and complex task. There is enormous opportunity in EDA Tools development and updating using AI/ML, to make decisions quicker, smarter and processes automate for large and complex VLSI circuits at different level of design and manufacturing [13], [14]. These ML algorithms facilitates chip manufacturing process faster, efficient and make decision making automated.

This paper liquidizes the literature regarding the application of AI/ML algorithms across various abstraction levels in chip design and manufacturing. It showcases a comprehensive review of VLSI chip design, verification, and testing in conjunction with AI/ML techniques. This paper is organized as follows: section 2 discuss the basic of AI-ML algorithms and review articles on it. Basic VLSI design flow and AI-ML role at design, verification is discussed in section 3. AI-ML contribution at various level of abstraction for chip design relevant review papers are briefed in section 4. Strengths, opportunities and threads of using AI-Ml in VLSI domain is concluded in section 5.

2. BRIEF ON ARTIFICIAL INTELLIGENCE, MACHINE LEARNING, AND DEEP NEURAL NETWORK

In today's world, statistical learning is essential to almost all new area of research and technology. Every field has access to enormous amounts of data that may be utilised to train the model and predict the desired parameter. These learning techniques are useful in solving many real life problems. A machine may mimic human behavior thanks to AI technology. The two primary subsets of AI are ML and deep learning (DL) or DNN. Without requiring any particular step-by-step programming, the ML-DL algorithm uses the historical information to identify patterns between input and output. As shown in Figure 1, ML is a subset of AI and DL is the subset of ML. With each new tuple added as experience in the dataset, machine learns, experience added and prediction accuracy improves. ML can handle mostly structured and balanced data. Three main categories in which ML algorithms divided are: supervised learning, unsupervised learning, and reinforcement learning. In supervised learning, machine has knowledge of both inputs and output for every tuple in the dataset. In unsupervised learning, information about only input variables is available in the dataset. Dataset having few tuples with labels and few are unlabeled are solved using reinforcement or semi-supervised learning techniques.

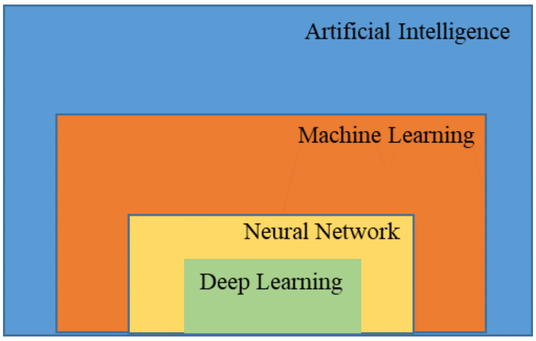

Figure 1. Relation of AI with other domains

2.1. Supervised learning

Supervised learning requires labeled data. With the knowledge of the correct output, ML model are either applied to solve regression problem or classification problem. Regression is the continuous value function. Missing or unseen data (numeric value) can be predicted using regression model. Classifier is the model, which predicts whether each example belong to which class. It helps in classifying (providing label to each tuple in the dataset) each example in the dataset, based on categorical information in the dataset. Prediction means numeric value for regression and label for classification problem. Y is a target variable (output), and x is the independent variable. ML model predicts the function f, which is defined as y=f(x). This mapping function approximate the output y for unseen input x. Obtaining a large, well-balanced dataset is a major obstacle when using supervised ML algorithms in the VLSI industry. Most widely used supervised ML algorithms are linear regression, logistic regression, ridge, lasso regression, and for classification decision tree, support vector machine (SVM), and random forest.

2.2. Unsupervised learning

Unlike supervised learning, unsupervised learning is not requiring output or labeled data. So, collecting data here is easier compared to supervised learning, but as required output is not known, it is harder to achieve final perfect results. Clustering is one of the applications of unsupervised learning, where classification of data points is done in different clusters. Based on input features, tuples with similarity are grouped together in a same cluster. Details of this is available at [15]. Dimensionality can be achieved through principal component analysis (PCA), unsupervised learning. Highly referred algorithms for clustering are K-nearest neighbors, K-means clustering, and hierarchical clustering [16].

2.3. Reinforcement learning

In reinforcement learning, machine makes decision and based on the result of the action, rewards are collected if the decision is correct, otherwise penalties are applied. This learning technique focuses on action-based, goal-directed learning [17]. In reinforcement learning technique, it does not depend on knowledge of correct output nor it search for the patterns in the data like supervised or unsupervised learning, rather it learns from feedback by environment by collecting maximum reward points.

2.4. Deep learning

DL is used to solve highly complex problem based on neural network. It identifies complex patterns within data and it helps in prediction and helps in solving real life problems like driverless car. It becomes increasingly popular due to availability of high processing power and readily available huge dataset. Main types of DL algorithm include convolutional neural networks (CNNs), recurrent neural networks (RNNs), radial basis function networks (RBFNs), multilayer perceptron (MLP), long short term memory networks (LSTMs) [18]. DNN translate low-level features to create high-level features by layer after another layer the attributes they extract, making them useful for finding distributed data expressions [19]. CNN involves mainly three steps convolution, nonlinear transformation and pooling. Convolution determines input features and identifies weights according to features and also shares weight values. Nonlinear transformation maps the input features using common functions as tanh, sigmoid, and rectified linear unit (ReLU). DNN has presently reshaped the computer vision industry. Computer vision problems are a good fit for DCNNs [20]. The generalized flow chart of “how DL algorithm works?”, is presented in Figure 2.

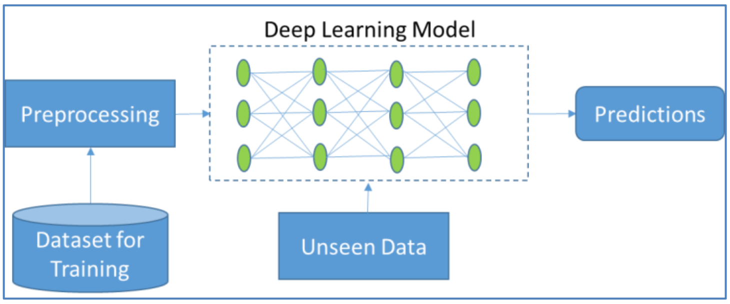

Figure 2. Work flow of DL model

3. ARTIFICIAL INTELLIEGENCE–MACHINE LEARNING IN VLSI DESIGN FLOW

This section provides a brief overview of approaches of ML, AI, and DL in physical design, layout, verification, and test pattern generation at different levels of abstraction and fault simulation.

3.1. Artificial intelligence-machine learning in very large scale integration chip design and physical design

First influence of AI in VLSI chip design was mentioned in 1985 [21]. AI methodologies and scope in CAD tool at several stages of VLSI design is discussed by the author and a quick overview of the available VLSI-AI technologies and a significance of including abilities of AI in CAD tools is described in detail. The effects of AI and intelligence systems on VLSI is discussed in details with benefits and drawbacks in [22]. They emphasized that AI will need to be incorporated into the entire VLSI design workflow, including the chip manufacturing process, interconnect technologies, packaging, design methodologies, and system architecture. As a result of the rapid advancements in AI/ML and latest algorithm development, researchers have focused on designing, developing, and applying AI/ML methodologies to VLSI design, verification and testing. Neural network usage in analog and digital circuit implementations are discussed in [23]. The integration of VLSI circuits with AI is explore and highlighted VLSI’s utilization of advanced semiconductor technology to facilitate diverse computer system functions. It focuses the close relationship between microelectronics and AI, proposing that the fusion of VLSI technology enables the creation of highly dynamic computer architectures. Using both data analytics and ML, physical design of the chip can be optimized. The challenges posed by the end-of-Moore scaling by analyzing data information flows in the IC design-to-manufacturing pipeline are addresses and opportunities for integrating big data analytics and ML solutions are identified in [24]. Authors review the components of the eco-system and outlined prime data flows in the IC design-to-manufacturing chain, suggesting a quantitative definition of physical design space coverage to validate the application of data analytics and ML methodologies, specifically in design-technology-co-optimization (DTCO) and DFMTop of form.

ML algorithms like ANN and SVM imply in physical design process to improve the CAD tool capabilities are discussed in [25]. There are many potentials for CAD, VLSI design, and their intersection as a result of the growth of ML. Major difficulties of several CAD tool algorithms have been identified and its potential solution using ML is discussed in [26]. In particular, they analyze the asynchronous CAD support and pinpoint prospects for ML inside these processes because several of the existing ML accelerators have leveraged asynchronous design. Enabling and promoting EDA tools to function in the cloud offers an environment for gathering information from both finished designs and the design process itself, spanning various designs and users.

3.2. Artificial intelligence-machine learning in integrated circuit testing

IC testing is evaluated by showcasing several ML methodologies and offering suggestions for aspiring users [24]. The author stated that ML may not be treated as a black-box method. It requires specific domain related knowledge and decision making. ML methodology applied for alternate test, test compaction and fault diagnostics.

The ML is also equally applicable and important for IC testing. Rather than conventional testing methods, ML based testing can be used for prediction of faulty or fault free parts of the chips. Conventional testing uses costly external automatic test equipment (ATE) is time consuming, while ML based approach has inexpensive information and has very fast response. ML based techniques for IC testing predicts with similar accuracy. The emphasis in ML domain should be on reducing the prediction risk to acceptable levels or even completely eliminating it. To solve this issue, mix approach should be used. First, ML based decisions may be used for IC testing and gain the confidence of the predictions, if it is not trusted fully, then followed by conventional method for the result of testing the IC. To have benefit of DL techniques, large data set is required for accurate predictions of the results. The author discussed in several ML approaches used in the domain of physical design; lithographic process, mask synthesis, verification, yield enhancement; failure modeling, ageing analysis, power, and thermal analysis; and analog design [27].

Kipf and Welling [28] emphasized the ML application in the entire design flow of the chip. Recent advancement in AI-ML has the capability to change entirely the chip design processes. They explore current research in the fields of autonomous design space exploration, power analysis, VLSI physical design, and analog IC design using methods like deep CNNs and graph-based neural networks. In order to increase designer productivity and automate optimization chores, a future vision of an AI-assisted automated chip design workflow also discussed. Particularly, when it's challenging to model the precise purpose or limitations of the EDA optimizations, ML based techniques have ample opportunities. Deep reinforcement learning (DRL) might transform into a new versatile EDA algorithm, similar to genetic algorithms, simulated annealing. ML also helps in optimizing speed for tape out. DRL optimization loop to automatically search the design space for superior physical floor plans, placements, and timing restrictions that can produce comparable favorable outcomes for subsequent clock-tree synthesis and routing phases.

Publications of research papers in VLSI design with ML increases three fold during 2017 and 2018 [12]. Because of attention of researchers in ML, incorporating it in chip design and manufacturing processes, reduces designer's time and effort in spent in data analysis, and shortens the time to market. In manufacturing and yield enhancement, ML plays the role of automating regular operations so that designer can spend longer addressing the more challenging question: why, rather than what. Employing a ML methodology has several major effects, but the most significant one is requiring standardization of gathering data, data accessibility and success criteria.

A paper is presented in depth discussion of the state of the art in ML for CAD at various levels of abstraction like logic synthesis, physical design, lithography and manufacturing, testing, device modeling [29]. Suitable ML algorithm like generative adversarial network, CNN, SVM are used at different abstraction level of VLSI design cycle. Heuristic algorithms continue to rule the CAD domain, but ML has potential to fill this gap. Main challenges that need to be taken care when applying ML in CAD tool were discussed by the authors. The trend for ML with the CAD tool suggested that ML is more applied towards physical design and neural network implementations compare to rest abstraction levels. unresolved issues were additionally highlights when using machine leaning in VLSI design, including the combinatorial optimization issue, the scarcity of data needed to train the model and certain practical issues. However, the most recent five years of significant conferences and journals have been covered only in the reviews and descriptions.

ML summary is properly tabulated by the author for physical design, static timing analysis, IR drop predictions and logic synthesis, analog design, testing and verification as well diagnosis [30]. A simplified algebraic model is introduced for analyzing single input change (SIC) circuits and explores the relationship between SIC sequences and their generating circuits, establishing key properties and design considerations. Through this analysis, the authors develop a novel SIC circuit called seeded autonomous circular shift register (SACSR), capable of generating SIC sequences with more unique vectors, validated by experimental results using the ISCAS85 benchmark dataset [31]. A circuit, netlist or layout can be represented in graphical from. So, graph neural network can be used in EDA to solve various optimization problem at different abstraction level and improve the performance of EDA [32]. A novel strategy for graph learning to contribute to the EDA and other domain would be useful to solve combinatorial challenges. Fault simulation and response compaction techniques are discussed using HOPE on ISCAS 89 full scan sequential benchmark circuits, leveraging parallel fault simulation and heuristics to reduce simulation time for designing space-efficient support hardware in VLSI self-testing. Building on prior work with sequence characterization and response data compaction, the authors apply these concepts to efficiently design space compression networks for full scan sequential circuits using the HOPE fault simulator [33].

3.3. Artificial intelligence-machine learning in different level of abstractions

Recent years have seen a significant advancement and acceptance of reinforcement learning, one of the ML techniques, found the scope in the field of EDA, in both research and industry [34]. Hybrid RL with DNN is applied for macro placement of the chip, sizing of the transistor, as well as logic synthesis [35]. strenght, weakness, opportunity, and threats (SWOT) analysis of RL algorithm in EDA is also represented by the authors.

Current advancement in AI-ML, has open the gate for solving many diversified problems including challenges in the field of chip design, verification, manufacturing and testing. The "level of abstraction" touches to the degree of detail or complexity at which a system or design is represented or understood. In the context of VLSI design [36]–[38]. There are multiple levels of abstraction ranging from the high-level system functionality down to the detailed transistor-level implementation. Figure 3 represents the types and flow of level of abstraction in VLSI design process. In this paper, a literature survey of various papers [3], [4], [25], [39], [40] which presented developing on AI/ML algorithms for various level of VLSI design cycles is carried out. The summary of few AI-ML algorithms used for different level of abstractions in VLSI Design cycle is tabulated in Table 1.

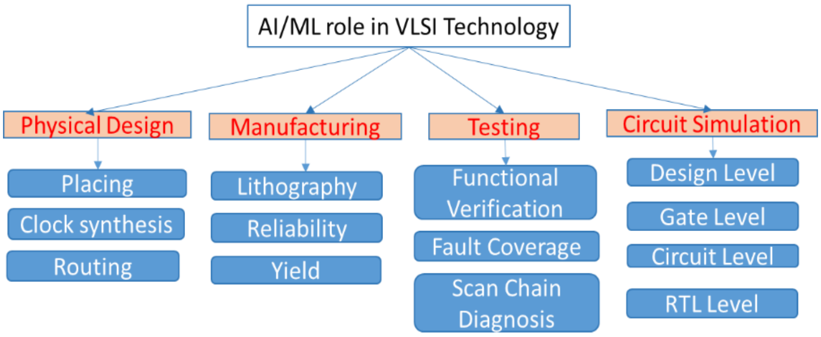

Figure 3. Role of AI/ML in VLSI design process

Table 1. List of AI-ML algorithms proposed in VLSI design flow

Sr. no	Level of abstraction in VLSI design	AI-Ml algorithm in reference
1	Design specification, architecture design, and verification.	LR, MARS, NN, SVM, NN, KNN, K-means, and GNN.
2	Netlist and formal verification.	PCA+NN, SVM, autoencoder, GCN, and NN [41], [42].
3	Floor planning, routing, clock tree synthesis, and layout verification.	GNN, CNN, SVM, CNN+SVM, LR, and RL [43], [44].
4	Lithography, packging, testing, and post silicon validation.	LR, SVM, NN, CNN, clustering+SVM, AdaBoost, clustering+autoencoder, autoencoder+GAN, decision tree, SGD, CGAN_CNN [45], and sparse encoder [46].

4. CONCLUSION

Many challenges so often occur in every aspect of designing, verification and testing of the chip due to shrinking in transistor dimensions. As a result, device become more sensitive to all the process variations consequently gain, leakage current and performance will deteriorate. A proper literature survey is carried out here, showcasing the role of AI, ML, and DL in VLSI technology, as well latest advancement carried out to reduce the process time. AI, ML, and various DL algorithms can lower the cost of testing a VLSI chips. On the contrary, fitting ML algorithms in classical VLSI design flow is the challenge task. Scarcity of data to train the model is solved, if industry understands the importance of using AI-ML in chip design flow. AI with ML can help in achieving optimization of VLSI design flow. The aim of this paper is to make the researchers aware about the algorithms developed for VLSI technology and could use the knowledge for specific design process in field of chip design.

REFERENCES

[1] J. -A. Carballo, W. -T. J. Chan, P. A. Gargini, A. B. Kahng and S. Nath, "ITRS 2.0: Toward a re-framing of the Semiconductor Technology Roadmap," *2014 IEEE 32nd International Conference on Computer Design (ICCD)*, Seoul, Korea (South), 2014, pp. 139-146, doi: 10.1109/ICCD.2014.6974673.

[2] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann and J. J. Welser, "Nanoscale CMOS," in *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537-570, April 1999, doi: 10.1109/5.752515.

[3] D. Amuru *et al.*, "AI/ML algorithms and applications in VLSI design and technology," *Integration*, vol. 93. p. 102048, 2023, doi: 10.1016/j.vlsi.2023.06.002.

[4] R. Vaddi, S. Dasgupta, and R. P. Agarwal, "Device and circuit design challenges in the digital subthreshold region for ultralow-power applications," *VLSI Design*, vol. 2009, 2009, doi: 10.1155/2009/283702.

[5] D. Sylvester and H. Kaul, "Power-driven challenges in nanometer design," in *IEEE Design & Test of Computers*, vol. 18, no. 6, pp. 12-21, Nov.-Dec. 2001, doi: 10.1109/54.970420.

[6] H. Iwai, "Logic LSI technology roadmap for 22 nm and beyond," *2009 16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, Suzhou, China, 2009, pp. 7-10, doi: 10.1109/IPFA.2009.5232710.

[7] B. H. Calhoun *et al.*, "Digital Circuit Design Challenges and Opportunities in the Era of Nanoscale CMOS," in *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343-365, Feb. 2008, doi: 10.1109/JPROC.2007.911072.

[8] M. H. Abu-Rahma and M. Anis, "Variability in VLSI circuits: Sources and design considerations," in *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343-365, Feb. 2008, doi: 10.1109/ISCAS.2007.378156.

[9] S. Chaudhuri and N. K. Jha, "FinFET logic circuit optimization with different FinFET styles: Lower power possible at higher supply voltage," *2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems*, Mumbai, India, 2014, pp. 476-482, doi: 10.1109/VLSID.2014.89.
[10] R. S. Rathore, A. K. Rana, and R. Sharma, "Threshold voltage variability induced by statistical parameters fluctuations in nanoscale bulk and SOI FinFETs," *2017 4th International Conference on Signal Processing, Computing and Control (ISPCC)*, Solan, India, 2017, pp. 377-380, doi: 10.1109/ISPCC.2017.8269707.
[11] A. R. Brown, N. Daval, K. K. Bourdelle, B. Y. Nguyen, and A. Asenov, "Comparative simulation analysis of process-induced variability in nanoscale soi and bulk trigate finfets," in *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3611-3617, Nov. 2013, doi: 10.1109/TED.2013.2281474.
[12] C. Schuermyer, "Deploying new nodes faster with machine learning for ic design and manufacturing," *2019 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, Hsinchu, Taiwan, 2019, pp. 1-3, doi: 10.1109/VLSI-TSA.2019.8804650.
[13] M. Belleville, O. Thomas, A. Valentian, and F. Clermidy, "Designing digital circuits with nano-scale devices: Challenges and opportunities," *Solid-State Electronics*, vol. 84, pp. 38–45, 2013, doi: 10.1016/j.sse.2013.02.030.
[14] L. Wang and M. Luo, "Machine learning applications and opportunities in IC design flow," *2019 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, Taiwan, 2019, pp. 1-3, doi: 10.1109/VLSI-DAT.2019.8742073.
[15] J. Franklin, "The Elements of Statistical Learning: Data Mining, Inference and Prediction," *Mathematical Intelligencer*, vol. 27, no. 2, pp. 83–85, 2005.
[16] N. E. H. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* vol. 53, no. 9. 2013.
[17] R. S. Sutton and A. G. Barto, *Reinforcement Learning, In The Lancet.* The MIT Press XtonBartoSecondBook, vol. 258, no. 6685. 1998
[18] S. Pouyanfar, "A Survey on Deep Learning: Algorithms, Techniques, and Applications," *ACM Computing Surveys (CSUR)*, vol. 51, no. 5, pp. 1–36, 2018, doi: 10.1145/323415.
[19] H. Yi, S. Shiyu, X. Duan, and Z. Chen, "A study on Deep Neural Networks framework," *2016 IEEE Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC),* Xi'an, China, 2016, pp. 1519-1522, doi: 10.1109/IMCEC.2016.7867471.
[20] E. Nishani and B. Cico, "Computer Vision Approaches based on Deep Learning and Neural Networks," *2017 6th Mediterranean Conference on Embedded Computing (MECO)*, 2017, pp. 11–14.
[21] C. K. C. Lee, "Deep Learning Creativity in EDA," *2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, Taiwan, 2020, pp. 1-1, doi: 10.1109/VLSI-DAT49148.2020.9196288.
[22] G. Rabbat, "VLSI and AI are getting closer," in *IEEE Circuits and Devices Magazine*, vol. 4, no. 1, pp. 15-18, Jan. 1988, doi: 10.1109/101.926
[23] M. Z. A. Khan, H. Saleem, and S. Afzal, "Application of VLSI In Artificial Intelligence," *IOSR Journal of Computer Engineering (IOSRJCE)*, vol. 6, no. 2, pp. 23–25, 2012, doi: 10.9790/0661-0622325.
[24] J. Liaperdos, A. Arapoyanni, and Y. Tsiatouhas, *Machine Learning in Alternate Testing of Integrated Circuits*, Springer International Publishing, 2019, doi: 10.1007/978-3-030-15628-2_16.
[25] L. Capodieci, "Data analytics and machine learning for design-process-yield optimization in electronic design automation and IC semiconductor manufacturing," *2017 China Semiconductor Technology International Conference (CSTIC)*, Shanghai, China, 2017, pp. 1-3, doi: 10.1109/CSTIC.2017.7919774.
[26] P. A. Beerel and M. Pedram, "Opportunities for Machine Learning in Electronic Design Automation," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5, doi: 10.1109/ISCAS.2018.8351731.
[27] M. Pradhan and B. B. Bhattacharya, "A survey of digital circuit testing in the light of machine learning," *WIREs Data Mining and Knowledge Discovery*, vol. 11, no. 1, pp. 1–18, 2021, doi: 10.1002/widm.1360.
[28] T. N. Kipf and M. Welling, "Semi-supervised classification with graph convolutional networks," in *5th International Conference on Learning Representations, ICLR 2017 - Conference Track Proceedings*, 2017.
[29] M. Rapp *et al.*, "MLCAD: A Survey of Research in Machine Learning for CAD Keynote Paper," *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 41, no. 10, pp. 3162-3181, Oct. 2022, doi: 10.1109/TCAD.2021.3124762.
[30] G. Huang *et al.*, "Machine Learning for Electronic Design Automation: A Survey," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 26, no. 5, 2021, doi: 10.1145/3451179.
[31] D. S. Lopera, L. Servadei, G. N. Kiprit, S. Hazra, R. Wille and W. Ecker, "A Survey of Graph Neural Networks for Electronic Design Automation," *2021 ACM/IEEE 3rd Workshop on Machine Learning for CAD (MLCAD)*, Raleigh, NC, USA, 2021, pp. 1-6, doi: 10.1109/MLCAD52597.2021.9531070.
[32] Y. Ma, Z. He, W. Li, L. Zhang, and B. Yu, "Understanding Graphs in EDA: From Shallow to Deep Learning," *ISPD '20: Proceedings of the 2020 International Symposium on Physical Design*, pp. 119–126, 2020, doi: 10.1145/3372780.3378173.
[33] S. R. Das, C. V. Ramamoorthy, M. H. Assaf, E. M. Petriu, W. Ben Jone, and M. Sahinoglu, "Fault simulation and response compaction in full scan circuits using HOPE," in *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 6, pp. 2310-2328, Dec. 2005, doi: 10.1109/TIM.2005.858102.
[34] S. Roy, S. K. Millican, and V. D. Agrawal, "Training Neural Network for Machine Intelligence in Automatic Test Pattern Generator," *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID)*, Guwahati, India, 2021, pp. 316-321, doi: 10.1109/VLSID51830.2021.00059.
[35] A. F. Budak, Z. Jiang, K. Zhu, A. Mirhoseini, A. Goldie, and D. Z. Pan, "Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives: (Invited Paper)," *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, 2022, pp. 500-505, doi: 10.1109/ASP-DAC52403.2022.9712578.
[36] J. Yu, Y. Li, X. Liu, and Z. Yang, "Machine learning in physical design," *Proceedings of the 2023 International Conference on Mathematical Physics and Computational Simulation*, 2023, pp. 144–150, doi: 10.54254/2753-8818/28/20230384.
[37] R. Karthick, A. Senthilselvi, P. Meenalochini, and S. S. Pandi, "An Optimal Partitioning and Floor Planning for VLSI Circuit Design Based on a Hybrid Bio-Inspired Whale Optimization and Adaptive Bird Swarm," *Journal of Circuits, Systems and Computers*, vol. 32, no. 8, 2023, doi: 10.1142/S0218126623502730.
[38] A. U. Qureshi and Er A. Bhargava, *Analysis & optimization of floor planning algorithms for vlsi physical design*, Concepts Books Publication, 2020.
[39] C. Tzeng and S. Huang, "UMC-Scan Test Methodology : Exploiting the Maximum Freedom of Multicasting," in *IEEE Design & Test of Computers*, vol. 25, no. 2, pp. 132-140, March-April 2008, doi: 10.1109/MDT.2008.55.
[40] Duan-Yang Liu *et al.*, "Machine learning for semiconductors," *Chip*, vol. 1, no. 4, p. 100033, 2022, doi: 10.1016/j.chip.2022.100033.

[41] B. V and R. J. Gowri, "Implementation Of Machine Learning In The Field Of VLSI Placement," *Journal of Emerging Technologies and Innovative Research*, vol. 10, no. 2, pp. 112–116, 2023.
[42] A. Agnesina, K. Chang, and S. K. Lim, "VLSI Placement Parameter Optimization using Deep Reinforcement Learning," *ICCAD '20: Proceedings of the 39th International Conference on Computer-Aided Design*, 2020, pp. 1-9, doi: 10.1145/3400302.3415690.
[43] Fu-Chieh Chang *et al.*, "Flexible Multiple-Objective Reinforcement Learning for Chip Placement," *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*, 2022, pp. 1392-1393, doi: 10.1145/3489517.3530617.
[44] A. Mirhoseini *et al.*, "Chip Placement with Deep Reinforcement Learning," *arXiv*, 2008, doi: 10.48550/arXiv.2004.10746.
[45] V. Alimisis, G. Gennis, M. Gourdouparis, C. Dimas, and P. P. Sotiriadis, "A Low-Power Analog Integrated Implementation of the Support Vector Machine Algorithm with On-Chip Learning Tested on a Bearing Fault Application," *Sensor*, vol. 23, no. 8, 2023, doi: 10.3390/s23083978.
[46] I. Hussein, L. Gaber, A. I. Hussein, and M. Moness, "Fault Detection based on Learning Deep Learning for Digital 2021 Gaber on Fault Detection based Deep Learning for Digital VLSI Circuits," *Procedia Computer Science*, vol. 194, pp. 122–131, 2021, doi: 10.1016/j.procs.2021.10.065.

BIOGRAPHIES OF AUTHORS

Sima K. Gonsai is currently working as an assistant professor in the Department of Electronics and Communication (EC) at L. D. College of Engineering, Gujarat, India. She has received B.E. in EC Engineering from U. V. Patel College of Engineering in 2004 and M.E. in EC with a specialization in Communication Systems Engineering from the L. D. College of Engineering, Gujarat, in 2007. She can be contacted at email: simagonsai@ldce.ac.in.

Kinjal Ravi Sheth is an assistant professor at L. D. Collage of Engineering, Ahmedabad, Gujarat, India since 2011. She has completed Ph.D. in the area of Machine Learning and Image Processing from Atmiya University at Department of Electronics and Communication, Rajkot, Gujarat, India in 2023. She has completed her Master of Engineering from Dharmasinh Desai University, Nadiad in 2008. Her area of interest is image processing, machine learning, and satellite communicaton. She can be contacted at email: krsheth@ldce.ac.in.

Dhavalkumar N. Patel had completed B.E. in Electronics and Communication Engineering from Ahmedabad Institute of Technology, Ognaj Ahmedabad in 2009. Completed M.E. in 2016 from Vishvakarma Government Engineering College, Chandkheda in Signal Processing and VLSI Technology (EC). Currently persuing Ph.D. from Sakalchand Patel University, Mehsana, Gujarat. At present, working as an Assistant professor in L. D. College of engineering and having 13 years of teaching experience. He can be contacted at email: dnpatel@ldce.ac.in.

Hardik B. Tank had completed B.E. in Electronics and Communication Engineering from Nirma University, Ahmedabad in 2009. Completed M.E. in 2019 from L. D. College of Engineering Ahmedabad in Communication Systems Engineering. Currently persuing Ph.D. from Sakalchand Patel University, Mehsana, Gujarat. At present, working as an assistant professor in L. D. College of Engineering and having 13 years of teaching experience. He can be contacted at email: hbtank@ldce.ac.in.

Hitesh L. Desai is an assistant professor at L. D. College of Engineering, Ahmedabad, Gujarat, India since 2020. He has completed M. Tech. in Electronics and Communication Engineering in 2012 from Ganpat University, Mehsana, Gujarat, India. His area of interest are antennas, digital signal processing, and communication systems. He can be contacted at email: hldesai21@gmail.com.

Shilpa K. Rana had completed B.E. in Electronics and Communication Engineering from CITC, Changa, Gujarat University, in 2008. Completed M.E in 2014 from Dharamsinh Desai University in Communication system Engineering. Currently persuing Ph.D. from Gujarat Technological University, Ahmedabad, Gujarat. At present, working as an Assistant professor in Government Engineering College, Modasa and having 14 years of teaching experience. She can be contacted at email: shilpa.rana@gecmodasa.ac.in.

Suresh Laxmanbhai Bharvad had completed B.E. in Electronics and Communication Engineering from Ahmedabad Institute of Technology, Ognaj Ahmedabad in 2009. Completed M.E in 2013 from Vishvakarma Government Engineering College, Chandkheda in Signal Processing and VLSI Technology (EC). Currently persuing Ph.D. from GTU, India. Working as Assistant Professor in LDCE since last 12 years. He can be contacted at email: slbharvad@gmail.com.