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# Arrhythmia classification using CMF-AFF based on electrocardiogram in field programmable gate array device

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**ABSTRACT**

Arrhythmia classification is categorization of irregular heart rhythms depending on patterns detected in electrocardiogram (ECG) signals assist in treatment and diagnosis of cardiac conditions. ECG evaluates heart's electrical activity to diagnose various heart conditions, but it is affected by interference or noise. ECG's signal filtering is essential pre-processing stage that minimizes noise and highlights wave characteristics in ECG data. However, digital filters are normally constructed by multiplying coefficient and then multiplying value given as feedback which leads to more power and area consumption. To solve these issues, coefficient memory compression (CMC) technique is proposed with an adaptive FIR filter (AFF) to achieve low area and low power dissipation by compressing memory requirements in a field programmable gate array (FPGA). An adaptive FIR filter is employed to effectively minimize noise like baseline noise, muscle contraction noise, and low-frequency noise. The performance of CMC-AFF is analyzed in terms of look up table (LUT), register, digital signal processing (DSP), power, and global buffer (BufG). The proposed approach achieves a low power consumption of 0.012 W in Zed Board Zynq7000 AP system on chip (SoC) FPGA device compared to existing techniques like collateral and sequence approaches using Bartlet filter and low-power ECG processor using Bartlet filter respectively.



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## 1. INTRODUCTION

Heart disease ranks among the top ten causes of death globally. An early warning system is essential for cardiac disease to efficiently minimize mortalities from cardiac death [1]. Cardiac arrhythmia is characterized by irregular heartbeats and requires continual treatment and monitoring due to its potential to result in cardiac arrest or stroke [2]. An electrocardiogram (ECG) is employed to visualize the electrical activity of the heart which provides a significant data source and its simplicity allows for easy monitoring and interpretation [3]. The traditional diagnosis involves identifying various kinds of arrhythmia to analyze the appropriate treatment strategies [4]. The QRS complex is predominant compared to all the ECG signal components [5]. ECG has various kinds of waves like P, T, and QRS waves. These waveforms are evaluated to identify the presence of the cardiac disorder. The popular significant data in ECG waveform is identified in the P wave morphology, T wave, and QRS complex [6]. ECG signal's P and T waves cause false detections while determining the QRS complex which leads to the establishment of detection approaches that depend on

mathematical morphology, band-pass filter, and wavelet transforms [7]. Unique integration of performance, flexibility, and energy efficiency produces an field programmable gate array (FPGA) that plays a vital role in accelerating computations in different domains like biomedical engineering [8]. FPGAs use pipeline or parallel execution of tasks, which decreases power consumption by employing a slower system clock [9]. Utilizing an AFF for denoising allows signal preprocessing without prior knowledge of the nature of noise [10], [11]. There are various classes in arrhythmia fibrillation, bradycardia, paced beat (PB), tachycardia, right bundle branch block (RBBB), and left bundle branch block (LBBB) [12]. Within these classes of arrhythmia, certain types can lead to life-threatening scenarios for cardiac patients. The implementation of FPGA-based ECG classification is developed earlier by utilizing a generator system for categorizing the ECG [13]. Compressing ECG data minimizes the transmitter signal time by transmitting fewer bits due to compression [14]. The usage of FPGA in filtering for arrhythmia classification generates improved signal processing abilities with low latency. Filtering indicates a promising solution to enhance the reliability and effectiveness of the arrhythmia classification system. FPGA generates effective and accurate detection of cardiac regularities which is essential for timely intervention and diagnosis [15]. However, digital filters are normally constructed by multiplying the coefficient, and then multiplied value is given as feedback which causes more power consumption and area. Kirti *et al.* [16] implemented collateral and sequence approaches that utilize Bartlett filter with windows and wavelet methods in FPGA. This approach generates the pre-processing phase in two stages: coefficient selection and filter architecture. This architecture uses three kinds of filters: notch filter, low pass filter (LPF), and high pass filter (HPF) to remove the base line wandering (BLW), power line interference (PLI), and electromyography (EMG) noise. The collateral approach reduces the usage of resources by sharing computation among various tasks and sequence techniques optimize FPGA performance in a coordinated manner. However, the collateral and sequence approaches utilizing the Bartlett filter suffer from higher resource utilization due to the simultaneous processing of multiple windows and wavelets.

Ahmad and Zafar [17] presented a quantized-pruned (QP) ID convolutional neural network (CNN) on system on chip (SoC) by utilizing high-level synthesis for machine learning (HLS4ML) for 3-channel ECG arrhythmia classification. HLS4ML provides two quantization approaches: quantization aware waiting (QAT) and post-training quantization (PTQ) which contain heterogenous model weight quantization. This heterogenous quantization through QAT with tunable precision optimizes fixed-point precision for various 1D CNN by effectively employing precision as a hyperparameter. However, the QP-1DCNN lacks hardware inefficiency due to the integration of specialized hardware for quantization and pruning strategies. Tripathi *et al.* [18] suggested a low-power ECG pre-processor using a Bartlett filter to extract the appropriate data from biomedical signals. A low-power pre-processing technique was designed for denoising the ECG. The LPF, HPF, and notch filter were utilized to eliminate the noise of EMG, BLW, and PLI respectively. All three types of filters were constructed by employing primary components comprised of multipliers, adders, and delay units. This approach focuses more on the benefits of FIR in effectively extracting valuable data from ECG signals which generates increased resourcefulness, and capabilities of rapid processing for signal analysis. However, low-power ECG pre-processor using a Bartlett filter has constraints like ringing effects during the initial stage of signal processing, the static nature of power, and increased memory usage. Tang *et al.* [19] introduced a second-order level-crossing sampling analog-to-digital (ADC) converter for ECG delineation and heartbeat detection of arrhythmia using a fiducial points pruning (FPP) filter. The delineation technique utilizes a triangle filter to determine the fiducial points and evaluates the slopes, intervals, P/T waves, and QRS complex morphology. Then, those extracted features were employed in heartbeat detection of arrhythmia to determine premature ventricular contraction (PVC). This approach greatly minimizes computing overhead for digital processing, communication circuits, and storage in the low-power system of data acquisition by employing ADC and ECG processing techniques. However, second-order level-crossing sampling ADCs were prone to signal distortion and noise due to the increased complexity of the sampling circuit. Elbedwehy *et al.* [20] developed an FPGA-based single node reservoir computing (SNRC) for ECG denoising using a cumulative mean filter. Initially, SNRC architecture was utilized to clean the decomposed ECG signal with high performance. A cost-effective, portable FPGA device was designed to combine privacy with high performance. The cumulative mean filter was employed to predict the recent value of the sample by averaging prior samples. This approach uses adders, SNRC, and multiples for fast signal summation, and signal processing which increases speed, power efficiency, and area utilization. However, the FPGA-SNRC has hardware constraints due to finite available resources in FPGA. In the overall analysis, it is indicated that existing methods have limitations like higher resource utilization due to simultaneous processing, static nature of power, and increased memory usage. To overcome this issue, the CMC-AFF is proposed to achieve low area and low power consumption by effectively compressing memory requirements.

The main contribution of this research is as follows: i) the CMC technique utilizes a 2's complement, Barrel shift, and addition module to efficiently minimize memory size which reduces area and

power consumption; ii) an AFF minimizes noise like baseline noise, muscle contraction noise, and low-frequency noise to achieve effective noise reduction; and iii) the main goal of the CMC-AFF is to evaluate with Virtex 7 xc7vx485t FPGA device for designing the 16-tap AFF. Additionally, CMF-AFF is evaluated with 2 FPGA devices such as Zed Board Zynq7000 AP SoC and Artix 7 XC7A100T.

The overall structure of the paper is as follows: section 2 contains the proposed method. Section 3 discusses a coefficient memory compression with adaptive finite impulse response filter. Section 4 indicates the results and discussion of the proposed method. Section 5 provides the conclusion.

## 2. METHOD

In this research, the CMC-AFF is proposed to reduce memory requirements which achieves low consumption of power and area. The obtained ECG signal is converted using analog to digital for the filtering process. The AFF is employed to remove noise like baseline noise, muscle contraction noise, and low-frequency noise. By using CMC technique, memory requirements are reduced with low power and power consumption by performing 2's complement, Barrel shift, and addition module. The QRS peaks are identified from filtered ECG signals and then features are extracted using a statistical analysis technique. Finally, naïve Bayes (NB) is developed to classify the heartbeat as normal or abnormal. Figure 1 represents the block diagram for the proposed approach.

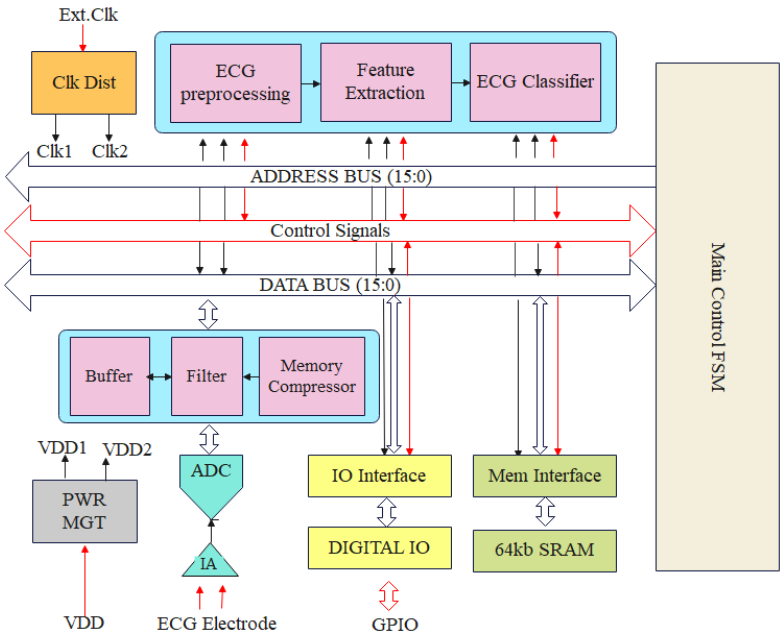



Figure 1. Block diagram for the proposed method

The process of the proposed CMC-AFF is presented as follows: i) initially, the ECG signal is obtained from MIT-BIH dataset to evaluate the proposed technique, and obtained signals are converted into analog to digital representation for filtering; ii) then, the AFF effectively minimizes noise like baseline noise, muscle contraction noise, and low-frequency noise by dynamically adjusting it is filter coefficients; iii) CMC technique utilizes a 2's complement, Barrel shift, and addition module to efficiently minimize memory size which reduces area and power consumption; iii) bandpass filtering is utilized to remove unwanted noise followed by QRS complex detection using PAT technique which analyzes ECG waveforms; iv) after detecting the QRS complex, the T and P waves are delineated depending on adaptive search windows with adaptive thresholds (ASW-AT) for distinguishing T and P peaks accurately from noise peaks; v) the final delineated waves are extracted using a statistical analysis approach. It extracts 7 features from ECG signals and forms them together to build a unique set; and vi) finally, the NB is utilized to classify the arrhythmia as abnormal or normal.

### 2.1. Electrocardiogram signal

In this research, the input ECG signals obtained from the standard Massachusetts Institute of Technology-Boston's Beth Israel Hospital (MIT-BIH) arrhythmia dataset [21] are utilized to evaluate the proposed approach. There are a total of 48 ECG records each has 30-minute durations. Every data employed here is sampled at a rate of 360 samples per second per channel with a resolution of 11-bit over a 10 mv range. These obtained signals are fed into the ADC converter to convert the signal into analog to digital. Table 1 provides data characteristics description for MIT-BIH dataset.

Table 1. Data characteristics description for MIT-BIH dataset

| Characteristics | Description |
|---|---|
| Number of patients | 47 |
| Number of recordings | 48 half-hour ECG recordings |
| Resolution | 11-bit |
| Sampling rate | 360 Hz |
| Channels | 2 channels |
| Data format | Standard ECG format with labeled beat annotations |
| Annotation | Detailed beat classification and arrhythmia occurrences |
| Noise level | Baseline noise, muscle contraction noise, and low-frequency noise |

### 2.2. Analog-to-digital converter

After obtaining the ECG signal from MIH-BIT, an ADC converter is utilized for converting continuous analog signals into digital representations for filtering that can be analyzed, processed, and manipulated by a microcontroller or microprocessor. This permits the FPGA to interface with analog and makes it interact with actuators, sensors, and other analog devices. The user program initializes the process of ADC conversion and it takes numerous microseconds to complete the conversion effectively. After converting an analog signal to digital, these signals are passed to an adaptive FIR filter to reduce noise effectively.

## 3. COEFFICIENT MEMORY COMPRESSION WITH ADAPTIVE FINITE IMPULSE RESPONSE FILTER

### 3.1. Adaptive FIR filter

Once ADC is performed, the digital signals are fed into an AFF which reduces noise like baseline noise, muscle contraction noise, and low-frequency noise. An adaptive filter is a filter with non-constant coefficients. Normally digital filters are constructed by multiplying the coefficients which requires more power and area. To solve these issues, an adaptive FIR filter is employed to reduce the consumption of power and area. The AFF filter doesn't need a multiplier, which uses only a shifting process, adder and 2's complement which minimizes the power consumption and area. The filter module effectively eliminates unwanted noise and frequency using a 64-tab MAC. Buffer stores the samples of ECG after digital conversion from ADC. Figure 2 shows the overall structure of the filter.

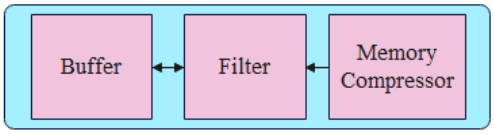



Figure 2. Structure of filter

#### 3.1.1. Memory compressor

The memory compressor contains four modules: address generator, memory module, 2's complement module, and barrel shift and addition module. The memory compressor generates the address in 16-bit by using 2's complement module. It has 0-15 addresses with a depth of 16-bit size. Normally, each bit requires an address for reading the data and then multiplying it with a coefficient for filtering operation which leads to computational overhead and increased processing time. To overcome this issue, 2's complement is used which eliminates the need for two memory locations. By using this, one location can effectively handle two data addresses. This research performs with coefficient compression utilizing 2's complement, Barrel shift, and addition module. This integrated technique generates a reduction in memory size to one-fourth of the windowing method. By input operand decomposition, this compression technique is

employed for the effective implementation of high-precision multiplication. It is determined that the ECG processor exhibits low area and time complexity for 16-bit word size. However, for higher word sizes, it has significantly less area and shorter multiplication time compared to canonical-signed-digit (CSD)-based multipliers. By using a memory compressor module, low power and area are effectively achieved. Figure 3 indicates the structure of the memory compressor module. The memory compressor with AFF is fed into the ECG pre-processing stage to reduce noise, to detect QRS, and T and P wave delineation.

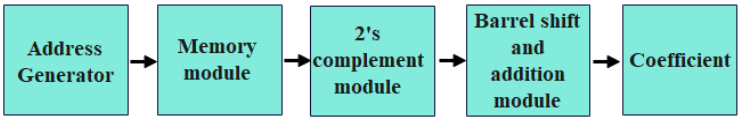



Figure 3. Structure of memory compressor module

### 3.2. ECG-preprocessing

After compressing the memory module, the pre-preprocessing phase is performed which contains three stages: filtering, detecting QRS, and delineation of T and P waves. Bandpass filtering is used to remove the unwanted noise from ECG signals. QRS detection is performed utilizing PAT technique to analyze ECG waveforms. The T and P waves are described depending on ASW-AT for distinguishing T and P peaks accurately from noise peaks.

#### 3.2.1. Filtering and QRS detection

Here, bandpass filtering [22] is utilized to remove the unwanted noise from the ECG signal which allows a certain range of frequencies to pass through blocking frequencies outside the range. This filter isolates relevant QRS energy at 10 Hz and attenuates the characteristics of a low frequency of P and T waves. By isolating the relevant frequency elements, the band pass filter eliminates both noises like low and high frequency noise. This results in a cleaner ECG signal which makes it easier to interpret and evaluate the underlying cardiac activity. The primary advantage is that it preserves data contained within an ECG signal even after filtering. QRS complex detection was performed once the unwanted noises were removed by using a bandpass filter. Accurate detection of QRS complex in ECG signals provides evaluation of heart rate and rhythm abnormalities which leads to an accurate diagnosis of arrhythmia. Here, the PAT technique is used to detect the QRS complex.

PAT is effective due to its adaptability to different ECG characteristics of a signal which generates robust performances and is suitable for accurate and effective arrhythmia analysis. It depends on amplitude threshold approach which exploits fact that the R peak has greater amplitude compared to other peaks in the ECG waveform. With appropriate signal filtering, this approach greatly detects the R peak in each heartbeat by utilizing two threshold levels. PAT approach contains four phases after filtering. Filtered signal differentiation is utilized to distinguish the complexities of QRS [23] from another wave by determining high slopes. Next, non-linear transformation is established via point-to-point squaring of ECG-filtered signal. This transformation is significant in highlighting high-frequency signals acquired from the prior phase which represents QRS's complex characteristics. Then, the integration is performed by moving the time window for extracting extra features like QRS width. At last, adaptive threshold amplitude is employed to average signal for detecting R peaks. Both average and bandpass filtered signals are stored in individual SRAM for further evaluation.

#### 3.2.2. T and P wave delineation

After detecting the QRS complex, the T and P waves are delineated depending on ASW-AT for distinguishing T and P peaks accurately from noise peaks. This approach can dynamically adjust to variations in ECG morphology which enhances robustness. QRS is utilized as reference to detect T and P waves in each heartbeat in that two regions are confined to R peaks. Then, these regions are employed to establish backward and forward search windows for T and P waves. Consider, that a forward search window has a T wave, and its boundary is increased from QRS offset to 2/3 of the priorly detected RR interval. Likewise, the P wave is determined and increased in a backward search window from QRS onset to 1/3 of prior RR interval. A position of T and P peaks are determined with associating search windows by evaluating local maxima/minima using corresponding thresholds which are expressed in (1) and (2).

$$T_{wave_{th}} = \frac{T_{peak}}{R_{peak}} t_{thresh_{in}} \quad (1)$$

$$P_{wave_{th}=\frac{P_{peak}}{R_{peak}}p_{thresh_{in}}} \quad (2)$$

where $t_{thresh_{in}}$ and $p_{thresh_{in}}$ indicates the T and P peak which is set between 0.1 and 0.2 depending on distinguished values in the window processing.

#### 3.2.3. Delineation of onset and offset point

ASW-AT hints a value of onset and offsets for P-QRS-T waves by determining sample that is associated with the ECG signal's zero slopes. A sample points have a former and zero slope to a peak which is recognized as an onset point. Likewise, an offset is identified by another peak side. Moreover, the change of derivative sign has occurred which represents a false indicator. To address this, adaptive search windows and threshold techniques incorporate other criteria to accurately delineate wave boundaries depending on fiducial points. These criteria are often combined with isoelectric lines. The line of isoelectric is approximated as the beat signal's average value after eliminating QRS complex. It is established and integrated with zero slopes to reliable and fiducial point accurate delineation. Before pre-processing, the ECG signal has significant noise which makes 30%-50% of the overall signal including baseline noise, muscle contraction noise, and low-frequency noise. After pre-processing, the noise level is minimized by 70-90% using filtering approaches leaving only 5-15% of signal affected by noise. After point delineation, feature extraction is performed to choose the best discriminative ECG features. Table 2 determines the data characteristics after pre-processing

Table 2. Characteristics for after pre-processing

| Characteristics | After pre-processing |
|---|---|
| Number of patients | remains same-47 |
| Number of recordings | remains same-48 half-hour ECG recordings |
| Resolution | remains same-11-bit |
| Sampling rate | remains same-360 Hz |
| Channels | remains same-2 channels |
| Data format | Same format with minimized noise and enhanced signal quality |
| Annotation | Detailed beat classification and arrhythmia occurrences |
| Noise level | Significantly minimizes noise after filtering |

### 3.3. Feature extraction

After performing onset and offset point delineation, a statistical analysis approach is employed to extract the features by considering complexity for arrhythmia classification. A statistical analysis approach is utilized to provide a balance for complexity and generate interpretable features that capture the variations and patterns in ECG signals with high efficiency and robustness. This approach extracts 7 features from ECG signals and forms them together to build a unique set. Every feature indicates various intervals from these signals, they are PQ, PS, RR, QP, TR, RT, and SP intervals. However, various features are required to increase the model's robustness. Hence, this unique set of ECG intervals is established. Finally, these unique feature sets are fed as input to a classification phase.

### 3.4. Classification

After extracting features, NB [24], [25] is utilized to determine the signal that is susceptible to ventricular arrhythmia. Compared to other techniques like support vector machine (SVM) and decision tree (DT), NB has a high potential with a p-value <0.001 in arrhythmia classification whether the heartbeat is normal or abnormal in ECG features. It determines the system performance without establishing significant bias in classification. NB is the simplest classification technique, requiring no complex estimation of iterative parameters. This enables it particularly helpful for the implementation of hardware. It considers strong naïve independent distributions among feature vectors, and these considerations are met since every extracted feature of ECG is independently assessed and analyzed from the starting stage. Bayesian classifier employs Bayes to determine data possibility for a specific class. Bayes theorem is expressed in (3) for a feature set vector $d$ and class $c_i$.

$$P\ (c_i|d) = \frac{P(d \mid c_i)\ P(\ c_i)}{p\ (d)} \quad (3)$$

Assigning data in the best class increases the probability of condition out of every class which are indicated in (4) and (5). Due to the risk of floating-point underflow, while calculating the product of the above probabilities, the point evaluation is transmitted into summation using logarithms. Instead of selecting

a class with the greatest probability, one with greatest log score is selected. Consider that log function is monotonic and decisions are identical which is formulated in (6). According to Gaussian, every feature vector value is connected with each distributed class. Therefore, the given value's conditional probability of $v$ from vector $x$ has a class of $c_i$, $P\ (v|c_i)$ is expressed in (7)-(9).

$$c = argmax\ P(c_i|d) \tag{4}$$

$$c = argmax\ P(c_i) \prod_x P(x|\ c_i) \tag{5}$$

$$c = argmax\ [\log(P(\ c_i)) + \sum_X \log(P\ (x|c_i))] \tag{6}$$

$$P\ (x = v|c_i) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(v-\mu)^2/2\sigma^2} \tag{7}$$

$$\mu = \sum_{i=1}^{N}(x_i) \tag{8}$$

$$\sigma^2 = \frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2 \tag{9}$$

Where $\mu$ and $\sigma^2$ are mean and variance of $x$ connected with class $c_i$. Figure 4 represents a schematic diagram of three stages: pre-processing, feature extraction, and classification.

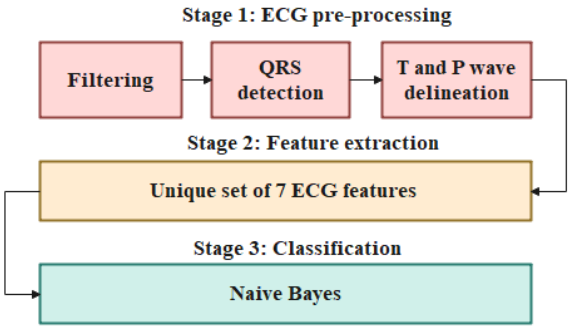



Figure 4. Schematic diagram of three stages

The probability log is computed by utilizing a LUT those entries are $\omega$-bit and $2^{\omega}$-bit deep. The LUT entries are indicated in 2's complement format. The Gaussian technique is constructed by calculating the above equations from each class training data for unclassified new values. This approach provides real-time processing with low power consumption and effective area utilization which enables it a significant solution for the effective arrhythmia classification diagnosis in FPGA. CMC effectively minimizes memory with the help of 2's complement, Barrel shift, and addition module which reduces low power consumption and area. AFF minimizes noise like muscle contraction noise, low-frequency noise, and baseline noise and achieves effective noise reduction. Therefore, the CMC-AFF technique reduces area utilization and power consumption by minimizing memory requirements and providing an effective filter design.

## 4. RESULTS AND DISCUSSION

The proposed CMC-AFF is simulated using Xilinx ISE 14.2 software. In this research, the Modelsim simulator is utilized to evaluate the adaptive FIR filter functional simulations. The main goal of the proposed technique is to utilize with Virtex 7 xc7vx485t FPGA device to design a 16-tap AFF. Additionally, CMC-AFF is evaluated with 2 FPGA devices Zed Board ZYNQ7000 and Artix 7 XC7A100T. The proposed memory compressor with 2's complement requires only one memory location instead of two different memory locations which assists in acquiring data from two different addresses. The AFF filter doesn't need a multiplier which uses only a shifting process and it contains an adder in a filter. Accordingly, the proposed memory compressor minimizes hardware utilization. The performance and hardware utilization are presented in the following subsections.

### 4.1. Performance analysis

The performance of CMC-AFF is evaluated using three different FPGA devices. The proposed technique is evaluated to LUT, FF, DSP, I/O, global buffer (BUFG), and power (mW). Figures 5 and 6 determine the abnormal or normal performances for arrhythmia classification. ECG signals from the MIT-BIH dataset undergo a filtering process that removes the noise from it. Then, the QRS complex is detected and extracted utilizing a statistical analysis. At last, arrhythmia classification is performed utilizing NB to classify the heartbeat as abnormal or normal which is shown in Figure 5.

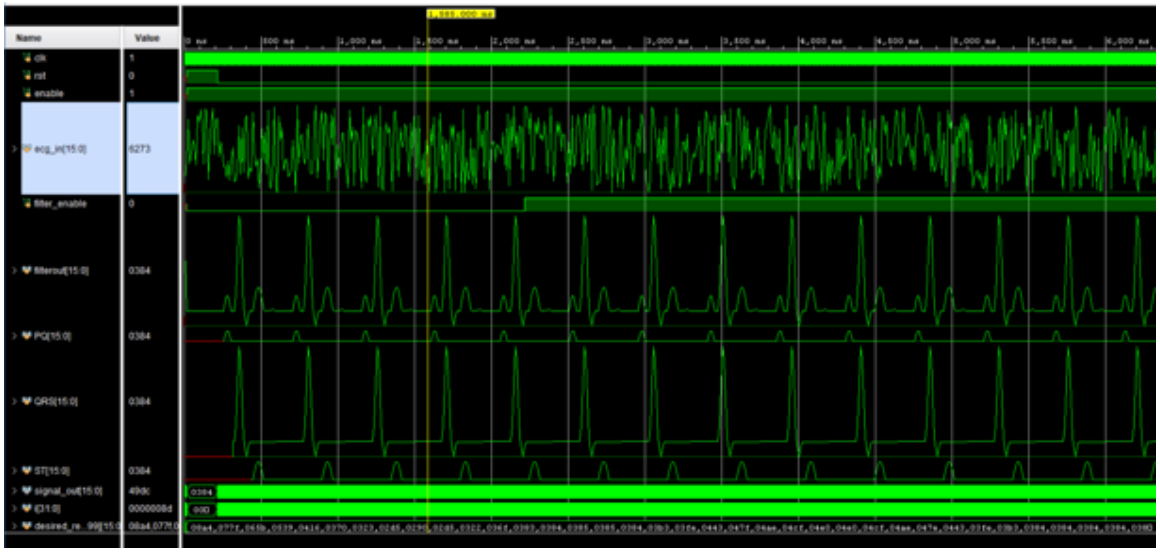


Figure 5. Abnormal signal for arrhythmia classification

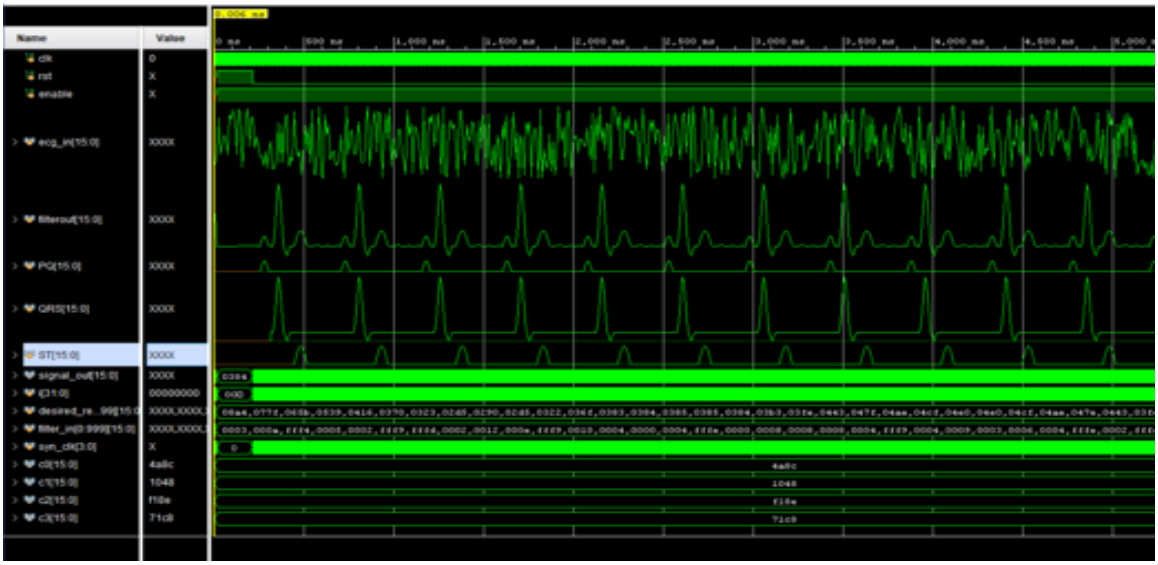
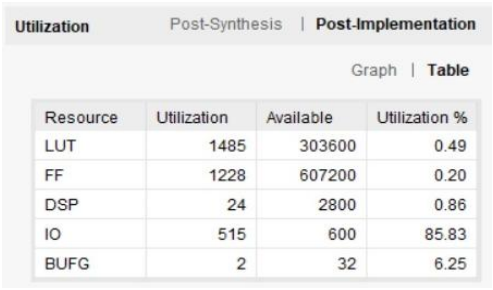


Figure 6. Normal signal for arrhythmia classification

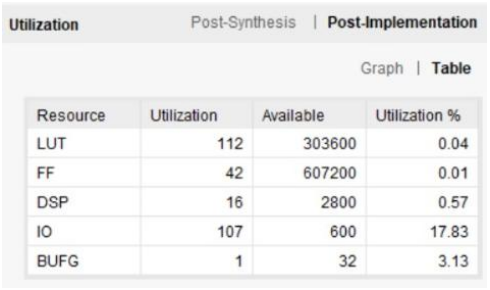
Figure 7 represents the hardware utilization of conventional digital filter performance for Virtex 7 xc7vx485t FPGA device without compressing memory coefficient. From this evaluation, it is concluded that the conventional digital filter performance of LUT, FF, DSP, I/O, and BUFG are employed between 0.20% to 85.83% of resources in the overall analysis. Figure 8 indicates the hardware utilization of CMC-AFF for the Virtex 7 xc7vx485t FPGA device. CMC-AFF occupies resource utilization between 0.01 to 17.83% which achieves less performance because of compressing memory coefficient compared to conventional digital filter performance.


Utilization Post-Synthesis | Post-Implementation

Graph | Table

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 1485 | 303600 | 0.49 |
| FF | 1228 | 607200 | 0.20 |
| DSP | 24 | 2800 | 0.86 |
| IO | 515 | 600 | 85.83 |
| BUFG | 2 | 32 | 6.25 |

Figure 7. Hardware utilization of conventional digital filter for Virtex 7 xc7vx485t FPGA device


Utilization Post-Synthesis | Post-Implementation

Graph | Table

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 112 | 303600 | 0.04 |
| FF | 42 | 607200 | 0.01 |
| DSP | 16 | 2800 | 0.57 |
| IO | 107 | 600 | 17.83 |
| BUFG | 1 | 32 | 3.13 |

Figure 8. Hardware utilization of CMC-AFF for Virtex 7 xc7vx485t FPGA device

Figures 9 and 10 illustrate the conventional power and proposed power consumption for the Virtex 7 xc7vx485t FPGA device. This analysis, shows that CMC-AFF has a less static power consumption of 1.587 W compared to conventional static power consumption of 6.632 W respectively. The proposed technique achieves less power because of compressing memory coefficient using 2's complement, Barrel shift, and addition module which reduces memory size and achieves low power consumption.

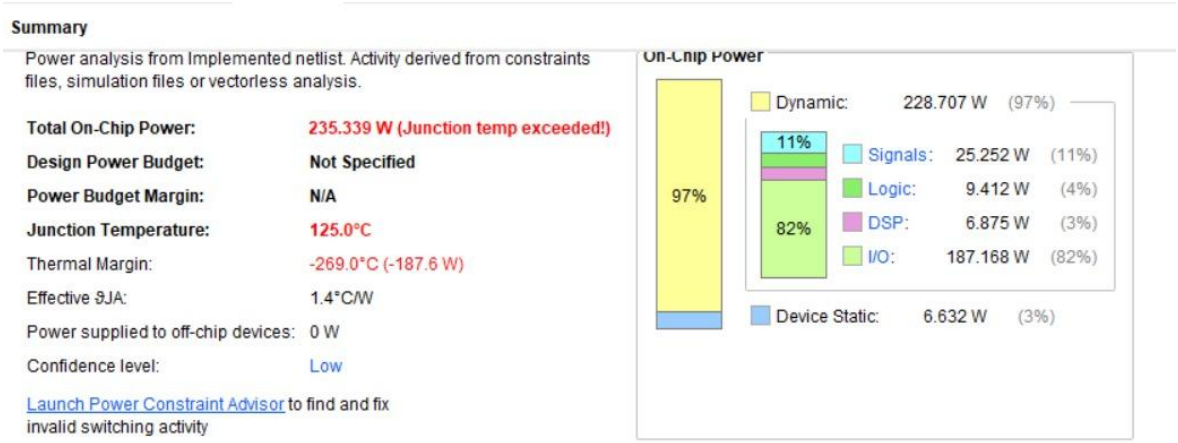



Figure 9. Power consumption of conventional digital filter for Virtex 7 xc7vx485t FPGA device

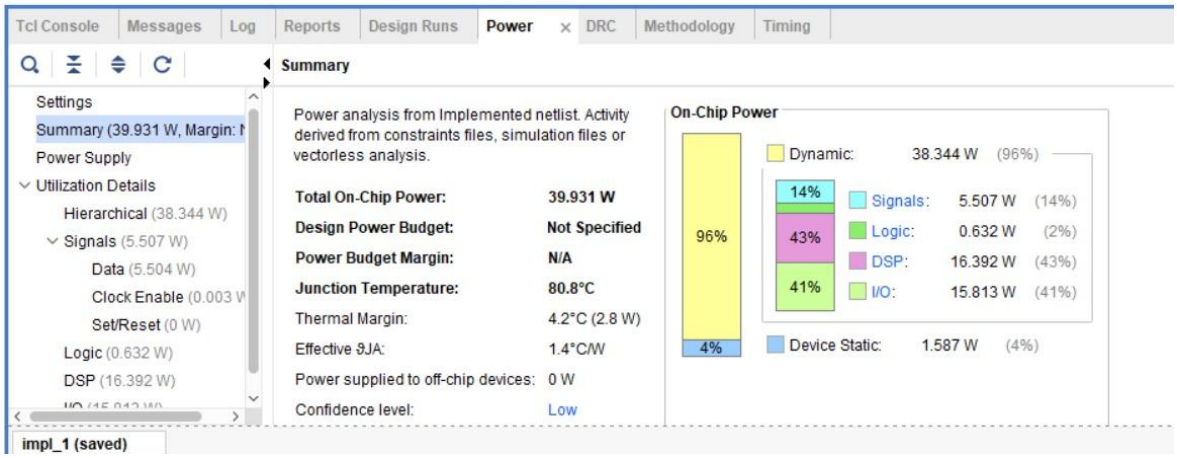



Figure 10. Power consumption of CMC-AFF for Virtex 7 xc7vx485t FPGA device

Tables 3 and 4 show hardware utilization of conventional digital filter performance and proposed CMC-AFF for Zed Board ZYNQ7000 FPGA devices. This analysis, clearly demonstrates that conventional digital filter performance utilizes between 0.795% to 37.500% of LUT, FF, DSP, I/O, and BUFG resources respectively. The proposed approach employs resource utilization between 0.287% to 23% which achieves less performance compared to conventional digital filter performances due to memory compression.

Table 3. Hardware utilization of conventional digital filter for Zed Board ZYNQ7000 FPGA device

| Resources | Utilization | Available | Utilization (%) |
|---|---|---|---|
| LUT | 628 | 53,200 | 1.180 |
| FF | 847 | 106,440 | 0.795 |
| DSP | 35 | 220 | 15.909 |
| I/O | 150 | 400 | 37.500 |
| BUFG | 2 | 26 | 7.692 |

Table 4. Hardware utilization of CMC-AFF for Zed Board ZYNQ7000 FPGA device

| Resources | Utilization | Available | Utilization (%) |
|---|---|---|---|
| LUT | 410 | 53,200 | 0.770 |
| FF | 306 | 106,440 | 0.287 |
| DSP | 12 | 220 | 5.454 |
| I/O | 92 | 400 | 23 |
| BUFG | 1 | 26 | 3.846 |

Table 5 represents hardware utilization of conventional digital filter performances for Artix 7 XC7A100T FPGA device. From this analysis, hardware utilization of conventional digital filter performances employs between 1.041% to 19.230% of LUT, FF, DSP, I/O, and BUFG resources. Table 6 indicates the hardware utilization of CMC-AFF for the Artix 7 XC7A100T FPGA device. CMC-AFF obtains less resource utilization between 0.615% to 11.538% compared to conventional digital filter performances because of the memory compressor.

Table 5. Hardware utilization of conventional digital filter for Artix 7 XC7A100T FPGA device

| Resources | Utilization | Available | Utilization (%) |
|---|---|---|---|
| LUT | 1,057 | 101,440 | 1.041 |
| FF | 1,123 | 106,440 | 1.055 |
| DSP | 35 | 220 | 15.909 |
| I/O | 40 | 400 | 10 |
| BUFG | 5 | 26 | 19.230 |

Table 6. Hardware utilization of CMC-AFF for Artix 7 XC7A100T FPGA device

| Resources | Utilization | Available | Utilization (%) |
|---|---|---|---|
| LUT | 650 | 101,440 | 0.640 |
| FF | 655 | 106,440 | 0.615 |
| DSP | 9 | 220 | 4.090 |
| I/O | 32 | 400 | 8 |
| BUFG | 3 | 26 | 11.538 |

Table 7 indicates power analysis for conventional digital filters and CMC-AFF using Zed Board ZYNQ7000 and Artix 7 XC7A100T. It shows that CMC-AFF achieves less power consumption of 0.012W and 45 mW compared to conventional digital filters for Zed Board ZYNQ7000 and Artix 7 XC7A100T FPGA devices. Because to AFF filter does not require a multiplier which uses only a shifting process, adder, and 2's complement operations, it significantly minimizes the power consumption.

Table 7. Analysis of power for conventional and CMC-AFF using two FPGA devices

| FPGA devices | Conventional digital filter | Proposed CMC-AFF |
|---|---|---|
| Zed Board ZYNQ7000 | 0.234 W | 0.012 W |
| Artix 7 XC7A100T | 90 mW | 45 mW |

### 4.2. Comparative analysis

Table 8 indicates the comparative analysis with existing methods for ZYNQ7000 FPGA device. The existing techniques like collateral and sequence approaches using Bartlett filter [16], and low-power ECG pre-processor using the Bartlett filter [18] are compared with a proposed technique for the Zed Board Zynq7000 AP SoC FPGA device. Compared to these existing techniques, CMC-AFF achieves a better LUT of 410, register of 850, DSP of 12, and power consumption of 0.012 W because of compressing memory coefficient. Table 9 represents the comparative analysis with existing methods for Artix 7 XC7A100T. SNRC with cumulative mean filter [20] is considered for the Artix 7 XC7A100T device. The proposed CMC-AFF is analyzed with and without pre-processing with the existing method [20]. When compared to this existing technique, the proposed CMC-AFF achieves 105 registers, 650 LUT, 3 BUFG, 9 DSP, and a power consumption of 45 mW respectively. Due developed AFF filter does not require a multiplier which uses only the shifting process in a filter which minimizes hardware utilization.

Table 8. Comparative analysis with an existing technique for Zed Board Zynq7000 AP SoC FPGA device

| Methods | LUT | Register | DSP | Power (W) |
|---|---|---|---|---|
| Collateral and sequence approaches using Bartlett filter [16] | 462 | 894 | 18 | 0.136 |
| Low-power ECG pre-processor using Bartlett filter [18] | 462 | 894 | 18 | 0.140 |
| Proposed CMC-AFF | 410 | 850 | 12 | 0.012 |

Table 9. Comparative analysis with the existing technique for Artix 7 XC7A100T FPGA device

| Methods | Pre-processing | Register | LUT | BUFG | DSP | Power (mW) |
|---|---|---|---|---|---|---|
| SNRC with cumulative mean filter [20] | Without pre-processing | N/A | N/A | N/A | N/A | N/A |
| | With pre-processing | 131 | 2938 | 1 | 12 | 82 |
| Proposed CMC-AFF | Without pre-processing | 128 | 1356 | 4 | 11 | 79 |
| | With pre-processing | 105 | 650 | 3 | 9 | 45 |

### 4.3. Discussion

In this section, the advantages of the proposed technique and the limitations of existing techniques are discussed. The existing techniques have limitations like Collateral and sequence approaches using Bartlett [16] suffer from higher resource utilization due to the simultaneous processing of multiple windows and wavelets. Low-power ECG pre-processor using Bartlett [18] has constraints like ringing effects during the initial stage of signal processing, static power consumption, and increased memory usage. FPGA-based SNRC using cumulative mean filter [20] has hardware constraints due to finite available resources in FPGA. The proposed CMC-AFF overcomes these existing techniques' limitations by compressing memory. The Bartlett filter and cumulative mean filter are static filters with fixed coefficients that have limited adaptability in varying noise. The proposed AFF filter doesn't need a multiplier, which uses only a shifting process, adder, and 2's complement which minimizes the power consumption. Hence, the CMC-AFF achieves less power consumption of 0.012 W for Zed Board Zynq7000 AP SoC FPGA devices compared to existing techniques respectively.

## 5. CONCLUSION

In this research, the CMC-AFF is proposed to achieve less power consumption and area during the filtering process. The memory coefficient with 2's complement eliminates the need for two memory locations that require only one location which effectively handles two data addresses. AFF reduces noises like baseline noise, muscle contraction noise, and low-frequency noise to achieve noise reduction. The filter doesn't need a multiplier which uses only a shifting process and incorporates an adder which minimizes hardware utilization. By performing these operations, the CMC-AFF achieves less power consumption of 0.112 W in Zed Board Zynq7000 AP SoC FPGA device compared to existing techniques like collateral and sequence approaches using Bartlet filter and low-power ECG processor using Bartlet filter respectively. In the future, an advanced filter architecture will be constructed to enhance the model performance.

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