Multi-objective optimization of CMOS low noise amplifier through nature-inspired swarm intelligence

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Article Info

Article history:

Received Dec 14, 2022 Revised Feb 2, 2023 Accepted Mar 24, 2023

Keywords:

180 nm complementary metal oxide semiconductor process Advance design system simulator Low noise amplifier circuit MATLAB environment MOABC algorithm MOPSO algorithm

ABSTRACT

This paper presents the application of two swarm intelligence techniques, multi-objective artificial bee colony (MOABC) and multi-objective particle swarm optimization (MOPSO), to the optimal design of a complementary metal oxide semiconductor (CMOS) low noise amplifier (LNA) cascode with inductive source degeneration. The aim is to achieve a balanced trade off between voltage gain and noise figure. The optimized LNA circuit operates at 2.4 GHz with a 1.8 V power supply and is implemented in a 180 nm CMOS process. Both optimization algorithms were implemented in MATLAB and evaluated using the ZDT1, ZDT2, and ZDT3 test functions. The optimized designs were then simulated using the advance design system (ADS) simulator. The results showed that the MOABC and MOPSO techniques are practical and effective in optimizing LNA design, resulting in better performance than previously published works, with a gain of 21.2 dB and a noise figure of 0.848 dB.

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INTRODUCTION

Almost all wireless communication applications use radio-frequency (RF) integrated circuits (ICs), such as low noise amplifiers (LNAs), in the RF receiver front end to amplify weak signals from receiving antenna to an appropriate level with lower noise. The two important factors that must be addressed when designing LNA are the noise figure and voltage gain [1]. Synthesizing low-noise amplifiers adequately requires many trade-offs between various performance objectives, including voltage gain, noise figure, power consumption, and others [2]. Generally, the main goal of LNA design is to simultaneously achieve two conflicting objectives: low noise figure and high voltage gain at given amount of power dissipation to meet the specification requirements.

Traditional analog design techniques are challenging when optimizing analog circuit characteristics, often requiring many redesign iterations and significant processing time, especially in complex designs where traditional methods may not provide optimal solutions. To overcome these challenges, designers have started using optimization algorithms such as simulated annealing (SA) [3], genetic algorithm (GA) [4]-[7], particle swarm optimization (PSO) [8]-[11], ant colony optimization (ACO) [12]-[17], and artificial bee colony algorithm (ABC) [18]–[21], to improve the design process and achieve desired performance in a reasonable time. However, analog circuit problems usually involve trade-offs between multiple performance characteristics, such as low noise figure and power consumption, stability and phase margin, or power consumption and resolution. Designers must balance these conflicting characteristics to achieve desired performance. For example, in bandpass filter design, there is a trade-off between selectivity and insertion loss. Similarly, oscillator design requires balancing frequency stability and power consumption. In amplifier design, power output must be traded off against distortion, while in ADC design, power consumption must be balanced with resolution.

The above-mentioned techniques have demonstrated their ability to search for optimal parameter, in many applications, including analog design, they can only address a single objective at a time, limiting their effectiveness. To address this limitation, multi-objective optimization algorithms have been developed to provide optimal solutions to design challenges involving multiple conflicting performance characteristics in analog circuits. These algorithms have become an increasingly popular solution to the challenges of analog circuit design [22], [23]. In this work, we describe and apply two of the most used swarm intelligence techniques: the multi-objective particle swarm optimization (MOPSO) and multi-objective artificial bee colony (MOABC) algorithms. We adapt and validate these algorithms through a benchmark of test functions before using them to optimize the voltage gain and noise figure of the RF complementary metal oxide semiconductor (CMOS) low-noise amplifier with inductive source degeneration as a multiobjective optimization problem.

The paper is structured as follows: section 2 provides an overview of the proposed MOABC and MOPSO algorithms. Section 3 discusses the performance validation of the optimization techniques using a benchmark test function. Section 4 describes the low-noise amplifier design. In section 5, we present the optimization results obtained using MATLAB software and the simulation results obtained using the advance design system (ADS) simulator. Finally, we conclude the paper.

2. AN OVERVIEW OF SWARM INTELLIGENCE TECHNIQUES

This section describes two of the most well-known and commonly used swarm intelligence techniques in the literature that belong to the family of metaheuristics inspired by nature. We will discuss the ABC and PSO algorithms, which will be presented in their multi-objective form.

2.1. Multi-objective artificial bee colony algorithm

Although it is a recent technique, the ABC algorithm is increasingly being used thanks to its innovative approach based on the population that has performed well when dealing with various optimization challenges [24]. The ABC algorithm simulates the foraging behavior of a bee swarm, where food sources correspond to potential solutions for an optimization problem. The nectar quantity of a food source indicates its quality as a solution. The ABC comprises employed, onlooker and scout bees. The ABC algorithm follows the main steps outlined:

a. Initialization phase

The scout bees randomly initialize the food source position and generate external archives by inserting the first non-dominated solutions.

b. Employed bee phase

Each employed bee locates a new source of nectar (sol_i*) in the vicinity of the current position of its food source (food_i). Therefore, by comparing the old and new solutions, the best one is chosen and saved in the archive using a greedy selection technique. The food source position is updated by the following equation:

$$sol_{i}^{j^{*}} = food_{i}^{j} + rand[-1; 1] * (food_{i}^{j} - food_{k}^{j})$$
 (1)

Where:

 $i \neq k$; $i \in (1,2,...,N)$; food^k represent the neighbor bee of food^j; j, k is randomly selected; N represents the number of employed bees.

c. Onlooker bee phase

The (food_i), is randomly chosen from the archive generated by the employed bee stage, and the greedy selection is applied to choose the best food source position. The new food source (sol_i^*) is produced by the following equation:

$$sol_{i}^{rp*} = food_{i}^{rp} + rand[-1; 1] * (AR_{k}^{rp} - food_{i}^{rp})$$
 (2)

Where:

 $k \in (1,2,...,m)$ is choosen randomly; while m, represent the archive size; rp is randomly selected from the archive. $i \in (1,2,...,Food number)$.

d. Scout bee phase

In case the solution cannot be improved after a limited number of tries, a scout bee occurs, and the food source position is updated by the following equation:

$$food_i = lb + rand[1; d] *. (ub - lb)$$
(3)

2.2. Multi-objective particle swarm optimization

Eberhart and Kennedy introduced PSO for the first time in 1995 [25]. It is a method inspired by nature, which studied the flocking behavior of birds. A set of particles is referred to as a swarm, and each bird is represented as a particle. Each particle in the decision space uses two types of velocities, pbest and gbest, where pbest is the particle's best location in history, and gbest is the swarm's best previously evaluated location. The PSO method begins by looking for uniformly distributed random solutions. If there are D decision variables, each particle can be represented by a D-dimensional vector, and the velocity (V_i) and current position (X_i) of the ith particle are represented as [26]:

$$X_{i} = \{x_{i1}, x_{i2}, \dots, x_{iD}\}$$
(4)

$$V_{i} = \{v_{i2}, \dots, v_{iD}\}$$
 (5)

The following information is used by each particle to attempt to change its position: i) current position, ii) distance between pbest and the current position, iii) distance between gbest and the current position, and iv) current velocities. The flowcharts of the proposed algorithms MOABC and MOPSO, are respectively described by the following Figures 1 and 2:

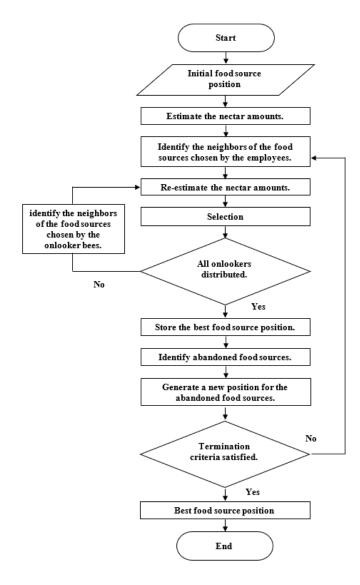


Figure 1. Flowchart of the MOABC algorithm

Figure 2. Flowchart of the MOPSO algorithm

The movement of the particle is controlled by updating its position and velocity of the ith particle according to the following expression:

$$V_{id}^{n+1} = \alpha \left(\omega. \, v_{id}^{n} + c_{1}. \, r_{1}^{n} (pbest_{id}^{n} - X_{id}^{n}) + c_{2}. \, r_{2}^{n} (gbest_{id}^{n} - X_{id}^{n}) \right) \tag{6}$$

With, i=1, 2, ..., N and d=1, 2, ..., D

$$X_i^{t+1} = X_i^t + V_i^{t+1} (7)$$

Where:

r1, r2 : random values between 0 and 1 c_2 : social acceleration coefficient

 $\omega \quad : intertia \ weight$

c₁ : cognitive acceleration coefficient
 gbest : global best of the particle
 pbest : personal best of the particle

ABC and PSO were adapted to be able to deal with multi-objective optimization problems (MO). Indeed, the goal of the MO approach is to generate a collection of solutions that are not dominated, which are referred to as Pareto optimal solutions for the problem [27]. The figures show the flowcharts of the proposed MOABC and MOPSO algorithms.

3. VALIDATION OF METAHEURISTICS PERFORMANCE BY TEST FUNCTIONS

To evaluate the performance of the two used algorithms, we chose a multi-objective benchmark consisting of three test functions known in the literature: Zitzler–Deb–Thiele's ZDT1, ZDT2, and ZDT3 [28]. The tests were performed using the MOABC and MOPSO control parameters listed in Tables 1 and 2. Figures 3(a)-(c) shows the pareto fronts of the benchmark test functions generated by the MOABC and MOPSO algorithms. It is clearly seen that the pareto fronts generated by the two proposed algorithms exactly match the true pareto fronts. As a comparison, the MOABC algorithm provides superior performance in terms of optimal quality compared to MOPSO. In fact, the MOABC shows a better distribution of solutions along the front with good regularity. These results show that the proposed optimization techniques can be applied to optimization problems with a guarantee of optimal convergence. In the following, the MOABC and MOPSO algorithms will be applied to the problem of optimal sizing of the LNA.

Table 1. Control parameters of MOABC algorithm

MOABC settings					
Max iteration	100				
Limit	100				
Dimension of the solution space (D)	4				
Size of the external archive (SAR)	25				
Number of colony size (NCS)	100				
Number of onlookers bees (%)	50				
Number of employed bees (%)	50				
Number of scouts (1)	1				

Table 2. Control parameters of MOPSO algorithm

MOPSO settings				
Dimension of the solution space (D)	4			
Max iteration 1	00			
Number of particles (NP)	00			
Size of the external archive (SAR)	25			
Weight damping rate (Wdamp) 0	.99			
Weight factor (w)	0.5			
Acceleration coefficient	1			
Acceleration coefficient	2			
Number of grids per dimension (NGrid)	7			
Inflation rate (α)	0.1			
Leader selection pressure (β)	2			
Deletion selection pressure (γ)	2			
Mutation rate (μ)	0.1			

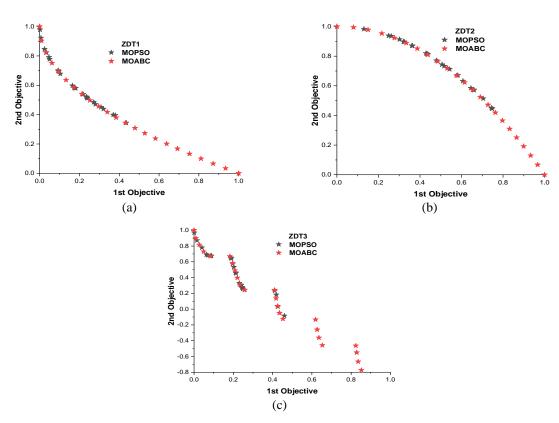


Figure 3. Pareto front of multi-objective test functions Pareto front of (a) ZDT1, (b) ZDT2, and (c) ZDT3

4. APPLICATION EXAMPLE: LOW NOISE AMPLIFIER DESIGN

4.1. Low noise amplifier circuit topology and analysis

The cascode topology with inductive source degeneration is the most widely used low-noise amplifier because it can simultaneously satisfy requirements for voltage gain and noise figure [29]. Figure 4(a) depicts the CMOS source inductive degeneration LNA topology, which uses inductive source

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degeneracy to represent an inductor (Ld) connected to the source of the M1 transistor. The cascading (M2) transistor minimizes the effect between the tuned output and input. The biasing circuit is implemented using an M3 transistor connected as a diode. Figure 4(b) illustrates the small-signal circuit of an LNA cascode amplifier, which is used for analyzing noise, including an intrinsic transistor noise model. The input matching network, represented by an inductor (Ls), determines the input impedance of the LNA. To maximize the output power transfer, the output inductor Ld is used to resonate with the output load [30].

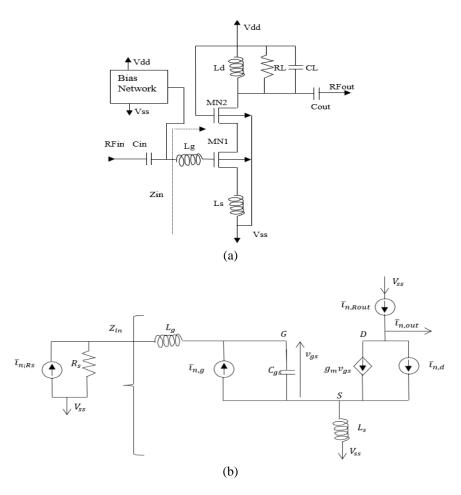


Figure 4. CMOS LNA Schematic and Small Signal Equivalent Circuit (a) CMOS LNA schematic and (b) LNA small signal equivalent circuit

4.1.1. Noise figure of the used low noise amplifier circuit

The definition of noise factor is defined by the following equation:

$$F = \frac{\text{Total output noise power}}{\text{Output noise due to the input source}}$$
(8)

In order to determine the expression for noise figure, it is necessary to apply thermal noise theory analysis to identify four distinct noise sources. Subsequently, the impact of these four sources on the output noise power must be determined using small signal analysis. The impact of the common-gate transistor on noise and frequency response is disregarded, along with the parasitic resistances of its D, S, G, and B terminals [31], [32]. In this noise analysis, four sources of noise have been considered: i) the thermal noise of the source resistance ($\bar{\iota}_{n,Rs}$); ii) the thermal noise of the output resistance ($\bar{\iota}_{n,Rout}$); iii) the gate noise ($\bar{\iota}_{n,g}$); iv) the channel thermal noise ($\bar{\iota}_{n,d}$).

The impact of the cascode M2 transistor on the noise is insignificant when compared to the main M1 transistor. Furthermore, the noise from the MOSFET's source and bulk resistance is considered minimal and not taken into account for this analysis, as stated in references [33], [34]. The analysis focuses on the four primary noise sources that affect the output, namely $\bar{\iota}_{o,Rs}$, $\bar{\iota}_{o,d}$, $\bar{\iota}_{o,g}$, $\bar{\iota}_{o,Rout}$ respectively [35]. The noise sources expressions are summarized in Table 3.

2830 ISSN: 2302-9285

Table 3	Notes controse and	Outnut ratarrad	AVDPACCIONO
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Noise source	Expression	Output referred expression
R_s	$\overline{\iota^2}_{n,Rs} = 4kT {}^1\!/R_s \Delta f$	$\bar{\iota}_{n,o,Rs} = \frac{g_m}{(j2\omega_0 C_{tot})} \bar{\iota}_{n,Rs}$
$\bar{\iota}_{n,d}$	$\overline{\iota^2}_{n,d} = 4kT\gamma g_{d0}\Delta f$	$\bar{\iota}_{n,\mathrm{o},d} = -\frac{1}{2}\bar{\iota}_{n,d}$
$ar{\iota}_{n,g}$	$\overline{\iota^2}_{n,g} = 4kT\beta g_g \Delta f$	$\bar{\iota}_{n,o,g} = \frac{g_m}{(j\omega_0 C_{tot})} \frac{(1 - jR_s \omega_0 C_{tot})}{j2R_s \omega_0 C_{tot}} \bar{\iota}_{n,g}$
R_{out}	$\bar{\iota^2}_{n,Rout} = 4kT {}^1\!/_{R_{out}} \Delta f$	$\bar{\iota}_{n,o,Rs} = \bar{\iota}_{n,Rout}$
Correlation btw $\overline{\iota}_{n,d}$ and $\overline{\iota}_{n,g}$	***	$ \bar{\iota}^{2}_{n,o,corr} = \frac{g_{m}}{(2\omega_{0}C_{tot})}\sqrt{\bar{\iota}^{2}_{n,g}\cdot\bar{\iota}^{2}_{n,d}} $

As a result, the LNA noise factor is expressed as (9):

$$F = \frac{\overline{\iota^2}_{n,o,Rs} + \overline{\iota^2}_{n,o,d} + \overline{\iota^2}_{n,o,g} + \overline{\iota^2}_{n,o,corr} + \overline{\iota^2}_{n,o,Rout}}{\overline{\iota^2}_{n,o,Rs}}$$
(9)

Using the equations listed in Table 3, the noise factor at the resonance is obtaind as (10):

$$F = 1 + \frac{A + B + C + D}{E} \tag{10}$$

Where,

$$A = \left(\frac{1}{4}\right) * \gamma * g_{d0} \tag{11}$$

$$B = g_m^2 * {\binom{C_{gs}}{C_{tot}}}^2 * {(Q^2 + 1/4)} * {\beta/(5 * g_{d0})}$$
(12)

$$C = g_m * c * {\binom{C_{gs}}{C_{tot}}} * \sqrt{\frac{(\gamma * \beta)}{20}}$$
(13)

$$D = \frac{1}{R_I} \tag{14}$$

$$E = g_m^2 * R_s * Q^2 \tag{15}$$

With, the white noise factor, intrinsic gate capacitance, correlation coefficient, gate noise parameter, and the sum of Cgs, Cd, and parasitic capacitance are represented by, γ , Cgs, c, β , and Ctot, respectively.

The following equations provide the input quality factor Q at the resonance frequency ω_0 :

$$Q = \frac{1}{R_{tot}\omega_0 C_{tot}} \tag{16}$$

Where,

$$\omega_0 = \frac{1}{\sqrt{L_{tot}C_{tot}}}$$
 and $R_s = \frac{g_m L_s}{C_{tot}}$ (17)

The gm and gd0 are approximated by the following expression [36].

$$g_m = A_0 * L^{A_1} * W^{A_2} * I_d^{A_3} \tag{18}$$

$$g_{d0} = B_0 * L^{B_1} * W^{B_2} * I_d^{B_3}$$
(19)

The length, width, and drain current of MOSFET transistors are represented by L, W, and Id, respectively. A_0 =0.0423, A_1 =-0.4578, A_2 =0.5275, A_3 =0.4725, B_0 =0.0091, B_1 =-0.5637, B_2 =0.5305, B_3 =0.4695, γ =1.05 and β =3.8 are constants. Finally, the noise figure expression is given as follows:

$$NF = 10log_{10}(F) \tag{20}$$

4.1.2. Voltage gain of the low noise amplifier

The first stage provides the input impedance Zin of this architecture at the resonance, Figure 4(b):

$$Z_{IN} = j\omega \left(L_g + L_s\right) + \frac{1}{j\omega c_{gs}} + \frac{g_m L_s}{c_{gs}}$$
(21)

Where the input resistance is given by:

$$R_{in} = Re[Z_{in}] = \frac{g_m}{c_{qs}} L_s \tag{22}$$

And at the resonance frequency,

$$\omega^2 = (L_q + L_s)C_{qs} = 1 \tag{23}$$

The gain of LNA is given by the following equation:

$$Gain = \frac{V_{out}}{V_{in}} = \frac{-j\omega g_m L_d}{1 - \omega^2 C_{gs}(L_g + L_s) + j\omega g_m L_s}$$

$$(24)$$

Substitute (23) into (24):

$$Gain = \frac{V_{out}}{V_{in}} = \frac{-j\omega g_m L_d}{j\omega g_m L_s} = \frac{-L_d}{L_s}$$
 (25)

Where, the gate input inductor, the inductor source degeneration, the operating frequency, the transconductance, the source resistance and gate-source capacitance of M1 transistor, are represented by Ls, Lg, ω 0, gm, Rs and Cgs, respectively.

4.2. Low noise amplifier design method

The problem of sizing ICs is addressed through multi-objective optimization algorithms and a performance evaluator based on analytical equations. The optimization process generates new sets of design variables at each iteration, including the width and length of transistors, as well as the sizes of resistors, capacitors, inductors, and other components [37]. The design methodology used is described in Figure 5. Two objective functions, namely the voltage gain and noise figure of an LNA circuit, are optimized using MOABC and MOPSO optimization techniques. The voltage gain should be maximized, and the noise figure should be minimized to obtain a good trade-off while respecting the design constraints and target specifications [38], as shown in Table 4.

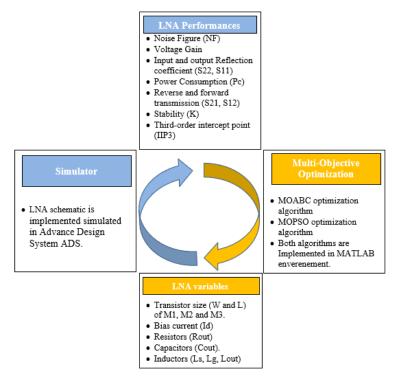


Figure 5. Flow diagram of LNA design method

Table 4. LNA specifications design						
Parameters	Specification					
Technology	CMOS 180 nm					
Power supply (Vdd)	1.8 V					
Bias current (Id)	<8 mA					
Power dissipation (Pd)	<=15 mw					
Operating frequency (F)	2.4 GHz					

<3 dB

>=10 dB

5. OPTIMIZATION AND SIMULATION RESULTS AND DISCUSSION

Noise figure (NF)

Voltage gain (S21)

5.1. Optimization results using MATLAB

The MOABC and MOPSO algorithms are applied to simultaneously optimize two objective functions of the LNA circuit: the voltage gains and noise figure. Therefore, the main goal is to minimize the noise figure (NF) and maximize the voltage gain to achieve a good trade-off. Both algorithms have been applied to generate the Pareto front, shown in Figure 6. Table 5 shows three random solutions chosen from the archive of results obtained by the MOABC and the MOPSO algorithms.

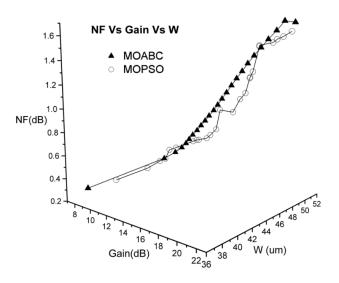


Figure 6. Pareto front of NF as function of gain and W

Table 5. Optimization results

MOABC algorithm							
Solutions	W (um)	L (um)	I (mA)	Gain (dB)	NF (dB)		
Sol@1	49.877	0.215	07.780	16.841	0.785		
Sol@2	50.000	0.220	06.137	15.593	0.906		
Sol@3	50.000	0.198	10.000	18.901	0.968		
		MOPSO	O algorithm				
Solutions	W (um)	L (um)	I (mA)	Gain (dB)	NF (dB)		
Sol@1	48.653	0.214	3.83	14.125	0.740		
Sol@3	46.511	0.209	3.95	14.730	0.692		
Sol@4	47.566	0.198	3.17	14.437	0.731		

5.2. Simulation results using advance design system

The ADS simulator is used to simulate the low-noise amplifier circuit to verify the required design performances and specifications. The resulting values obtained by the MOABC and MOPSO algorithms are applied as the design circuit parameters in the ADS simulator. The simulations are performed using CMOS 180 nm process with a 1.8 V power supply. Figures 7 and 8 show the LNA test bench and simulation results of voltage gain and noise figure as functions of frequency, respectively.

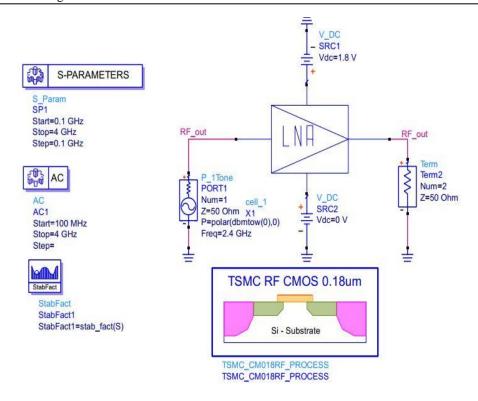


Figure 7. LNA test bench circuit

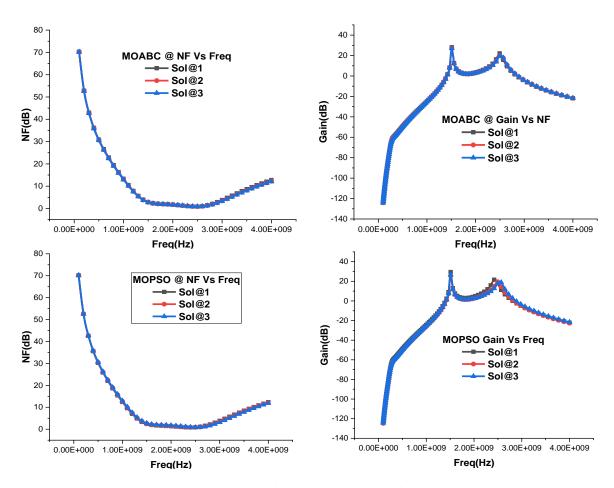


Figure 8. Simulation results of NF and gain as function of frequency of 3 solutions (sol@1, sol@2, sol@3)

Table 6 provides insights into the relative errors of the voltage gain and noise figure for two objective functions. The results suggest that the MOABC algorithm delivered the best trade-off solution (Sol@3) with the highest level of consistency between optimization and simulation outcomes. Furthermore, the MOABC algorithm's performance surpassed that of the MOPSO algorithm, as evidenced by the lower relative error values of 22.22% and 29.91%, respectively. Table 7 shows a comparison of the optimization results obtained by the MOABC and the MOPSO techniques and by the other ones reported in the literature [39]–[43]. Therefore, we can notice that the obtained LNA design has a low noise figure and a high voltage gain, compared to other techniques documented in literature.

Table 6. Optimization and simulation results

MOABC algorithm							
	MATLAB ADS			OS	Relative error*		
Solutions	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	%ErrGain	%ErrNF	
Sol@1	16.841	0.785	14.413	0.913	16.845	14.047	
Sol@2	15.593	0.906	12.758	0.938	22.222	03.374	
Sol@3	18.901	0.968	21.200	0.848	10.846	14.164	
	MOPSO algorithm						
	MATLAB ADS Relative error*						
Solutions	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	%ErrGain	%ErrNF	
Sol@1	14.125	0.740	14.060	0.885	00.462	16.395	
Sol@2	14.730	0.692	18.651	0.832	21.023	16.844	
Sol@3	14.437	0.731	20.599	0.816	29.914	10.447	

^{*}Relative error=100×|Opti. value-Sim. value|/Sim. Value

Table 7. Performances comparison

Parameter	[3	9]	[40]	[41]	[42]	[43]	This	work
Methods	ACO	ACO	Classic	Classic	Classic	GA	MOPSO	MOABC
Power supply (V)	2	2	1	1.8	1.2	1.8	1.8	1.8
Frequency (GHz)	2.3	2.3	2.4	2.4	2.4	1.5	2.4	2.4
Voltage gain (dB)	9.432	10.24	18.2	20.10	20	19.722	20.59	21.2
Noise figure (dB)	0.328	0.310	3.4	3.2	5.6	0.745	0.731	0.816

6. CONCLUSION

In this paper, we have presented an optimization approach for the optimal sizing of an LNA circuit. The proposed MOABC and MOPSO algorithms were adapted and successfully applied to maximize the voltage gain while minimizing the noise figure of the LNA circuit. The optimized design, implemented in a CMOS 180 nm process, operates at 2.4 GHz with a 1.8 V power supply. The proposed circuit design achieves a better trade-off between voltage gain and noise figure (Gain=21.200, NF=0.848) while consuming less power. The optimized designs were simulated using the ADS simulator to verify the validity of the results achieved by the algorithms. The optimization and simulation values were in agreement, showing the benefits of the proposed design methodology. The results are very promising for helping the designers reduce the number of redesign iterations by only selecting the best design for a specific application. Finally, the achieved LNA design shows better performance than other optimization-based methods previously reported in the literature.

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