Multi-objective optimization of CMOS low noise amplifier through nature-inspired swarm intelligence

Hamid Bouali¹, Bachir Benhala², Mohammed Guerbaoui¹
¹High School of Technology, Moulay Ismail University, Meknes, Morocco
²Faculty of Science Dhar El Mahrez, Sidi Mohamed Ben Abdellah University, Fez, Morocco

ABSTRACT
This paper presents the application of two swarm intelligence techniques, multi-objective artificial bee colony (MOABC) and multi-objective particle swarm optimization (MOPSO), to the optimal design of a complementary metal oxide semiconductor (CMOS) low noise amplifier (LNA) cascode with inductive source degeneration. The aim is to achieve a balanced trade off between voltage gain and noise figure. The optimized LNA circuit operates at 2.4 GHz with a 1.8 V power supply and is implemented in a 180 nm CMOS process. Both optimization algorithms were implemented in MATLAB and evaluated using the ZDT1, ZDT2, and ZDT3 test functions. The optimized designs were then simulated using the advance design system (ADS) simulator. The results showed that the MOABC and MOPSO techniques are practical and effective in optimizing LNA design, resulting in better performance than previously published works, with a gain of 21.2 dB and a noise figure of 0.848 dB.

Keywords:
180 nm complementary metal oxide semiconductor process
Advance design system simulator
Low noise amplifier circuit
MATLAB environment
MOABC algorithm
MOPSO algorithm

1. INTRODUCTION
Almost all wireless communication applications use radio-frequency (RF) integrated circuits (ICs), such as low noise amplifiers (LNAs), in the RF receiver front end to amplify weak signals from receiving antenna to an appropriate level with lower noise. The two important factors that must be addressed when designing LNA are the noise figure and voltage gain [1]. Synthesizing low-noise amplifiers adequately requires many trade-offs between various performance objectives, including voltage gain, noise figure, power consumption, and others [2]. Generally, the main goal of LNA design is to simultaneously achieve two conflicting objectives: low noise figure and high voltage gain at given amount of power dissipation to meet the specification requirements.

Traditional analog design techniques are challenging when optimizing analog circuit characteristics, often requiring many redesign iterations and significant processing time, especially in complex designs where traditional methods may not provide optimal solutions. To overcome these challenges, designers have started using optimization algorithms such as simulated annealing (SA) [3], genetic algorithm (GA) [4]–[7], particle swarm optimization (PSO) [8]–[11], ant colony optimization (ACO) [12]–[17], and artificial bee colony algorithm (ABC) [18]–[21], to improve the design process and achieve desired performance in a reasonable time. However, analog circuit problems usually involve trade-offs between multiple performance characteristics, such as low noise figure and power consumption, stability and phase margin, or power consumption and resolution. Designers must balance these conflicting characteristics to achieve desired performance. For example, in...
bandpass filter design, there is a trade-off between selectivity and insertion loss. Similarly, oscillator design requires balancing frequency stability and power consumption. In amplifier design, power output must be traded off against distortion, while in ADC design, power consumption must be balanced with resolution.

The above-mentioned techniques have demonstrated their ability to search for optimal parameter, in many applications, including analog design, they can only address a single objective at a time, limiting their effectiveness. To address this limitation, multi-objective optimization algorithms have been developed to provide optimal solutions to design challenges involving multiple conflicting performance characteristics in analog circuits. These algorithms have become an increasingly popular solution to the challenges of analog circuit design [22], [23]. In this work, we describe and apply two of the most used swarm intelligence techniques: the multi-objective particle swarm optimization (MOPSO) and multi-objective artificial bee colony (MOABC) algorithms. We adapt and validate these algorithms through a benchmark of test functions before using them to optimize the voltage gain and noise figure of the RF complementary metal oxide semiconductor (CMOS) low-noise amplifier with inductive source degeneration as a multiobjective optimization problem.

The paper is structured as follows: section 2 provides an overview of the proposed MOABC and MOPSO algorithms. Section 3 discusses the performance validation of the optimization techniques using a benchmark test function. Section 4 describes the low-noise amplifier design. In section 5, we present the optimization results obtained using MATLAB software and the simulation results obtained using the advance design system (ADS) simulator. Finally, we conclude the paper.

2. AN OVERVIEW OF SWARM INTELLIGENCE TECHNIQUES

This section describes two of the most well-known and commonly used swarm intelligence techniques in the literature that belong to the family of metaheuristics inspired by nature. We will discuss the ABC and PSO algorithms, which will be presented in their multi-objective form.

2.1. Multi-objective artificial bee colony algorithm

Although it is a recent technique, the ABC algorithm is increasingly being used thanks to its innovative approach based on the population that has performed well when dealing with various optimization challenges [24]. The ABC algorithm simulates the foraging behavior of a bee swarm, where food sources correspond to potential solutions for an optimization problem. The nectar quantity of a food source indicates its quality as a solution. The ABC comprises employed, onlooker and scout bees. The ABC algorithm follows the main steps outlined:

a. Initialization phase

The scout bees randomly initialize the food source position and generate external archives by inserting the first non-dominated solutions.

b. Employed bee phase

Each employed bee locates a new source of nectar (sol_i) in the vicinity of the current position of its food source (food). Therefore, by comparing the old and new solutions, the best one is chosen and saved in the archive using a greedy selection technique. The food source position is updated by the following equation:

\[
sol_i^* = food_i + \text{rand}[-1;1] \times (food_i - food_j)
\]

(1)

Where:

i \neq k; i \in (1, 2, ..., N); food_j^k represent the neighbor bee of food_i; j, k is randomly selected; N represents the number of employed bees.

c. Onlooker bee phase

The (food_i) is randomly chosen from the archive generated by the employed bee stage, and the greedy selection is applied to choose the best food source position. The new food source (sol_i*) is produced by the following equation:

\[
sol_i^{*P} = food_i^{*P} + \text{rand}[-1;1] \times (AR_i^{*P} - food_i^{*P})
\]

(2)

Where:

k \in (1, 2, ..., m) is chosen randomly; while m, represent the archive size; rp is randomly selected from the archive. i \in (1, 2, ..., Food number).

d. Scout bee phase

In case the solution cannot be improved after a limited number of tries, a scout bee occurs, and the food source position is updated by the following equation:

---

Multi-objective optimization of CMOS low noise amplifier through nature-inspired ... (Hamid Bouali)
\[ f_{ood_i} = lb + rand[1; d] \cdot (ub - lb) \] (3)

2.2. Multi-objective particle swarm optimization

Eberhart and Kennedy introduced PSO for the first time in 1995 [25]. It is a method inspired by nature, which studied the flocking behavior of birds. A set of particles is referred to as a swarm, and each bird is represented as a particle. Each particle in the decision space uses two types of velocities, pbest and gbest, where pbest is the particle's best location in history, and gbest is the swarm's best previously evaluated location. The PSO method begins by looking for uniformly distributed random solutions. If there are D decision variables, each particle can be represented by a D-dimensional vector, and the velocity \( V_i \) and current position \( X_i \) of the ith particle are represented as [26]:

\[ X_i = \{x_{i1}, x_{i2}, \ldots, x_{iD}\} \] (4)

\[ V_i = \{v_{i2}, \ldots, v_{iD}\} \] (5)

The following information is used by each particle to attempt to change its position: i) current position, ii) distance between pbest and the current position, iii) distance between gbest and the current position, and iv) current velocities. The flowcharts of the proposed algorithms MOABC and MOPSO, are respectively described by the following Figures 1 and 2:

![Flowchart of the MOABC algorithm](image-url)
Multi-objective optimization of CMOS low noise amplifier through nature-inspired ... (Hamid Bouali)

Figure 2. Flowchart of the MOPSO algorithm

The movement of the particle is controlled by updating its position and velocity of the ith particle according to the following expression:

\[ V_{id}^{n+1} = \alpha (\omega \cdot V_{id}^n + c_1 \cdot r_1^n (pbest_{id}^n - X_{id}^n) + c_2 \cdot r_2^n (gbest_{id}^n - X_{id}^n)) \]  

\[ X_{id}^{n+1} = X_{id}^n + V_{id}^{n+1} \]

With, \( i = 1, 2, \ldots, N \) and \( d = 1, 2, \ldots, D \)

Where:
- \( r_1, r_2 \) : random values between 0 and 1
- \( c_2 \) : social acceleration coefficient
- \( \omega \) : inertia weight
- \( c_1 \) : cognitive acceleration coefficient
- \( gbest \) : global best of the particle
- \( pbest \) : personal best of the particle

ABC and PSO were adapted to be able to deal with multi-objective optimization problems (MO). Indeed, the goal of the MO approach is to generate a collection of solutions that are not dominated, which are referred to as Pareto optimal solutions for the problem [27]. The figures show the flowcharts of the proposed MOABC and MOPSO algorithms.

3. VALIDATION OF METAHEURISTICS PERFORMANCE BY TEST FUNCTIONS

To evaluate the performance of the two used algorithms, we chose a multi-objective benchmark consisting of three test functions known in the literature: Zitzler–Deb–Thiele's ZDT1, ZDT2, and ZDT3 [28]. The tests were performed using the MOABC and MOPSO control parameters listed in Tables 1 and 2. Figures 3(a)-(c) shows the pareto fronts of the benchmark test functions generated by the MOABC and MOPSO algorithms. It is clearly seen that the pareto fronts generated by the two proposed algorithms exactly match the true pareto fronts. As a comparison, the MOABC algorithm provides superior performance in terms of optimal quality compared to MOPSO. In fact, the MOABC shows a better distribution of solutions along the front with good regularity. These results show that the proposed optimization techniques can be applied to optimization problems with a guarantee of optimal convergence. In the following, the MOABC and MOPSO algorithms will be applied to the problem of optimal sizing of the LNA.
Table 1. Control parameters of MOABC algorithm

<table>
<thead>
<tr>
<th>MOABC settings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Max iteration</td>
<td>100</td>
</tr>
<tr>
<td>Limit</td>
<td>100</td>
</tr>
<tr>
<td>Dimension of the solution space (D)</td>
<td>4</td>
</tr>
<tr>
<td>Size of the external archive (SAR)</td>
<td>25</td>
</tr>
<tr>
<td>Number of colony size (NCS)</td>
<td>100</td>
</tr>
<tr>
<td>Number of onlookers bees (%)</td>
<td>50</td>
</tr>
<tr>
<td>Number of employed bees (%)</td>
<td>50</td>
</tr>
<tr>
<td>Number of scouts (1)</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2. Control parameters of MOPSO algorithm

<table>
<thead>
<tr>
<th>MOPSO settings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension of the solution space (D)</td>
<td>4</td>
</tr>
<tr>
<td>Max iteration</td>
<td>100</td>
</tr>
<tr>
<td>Number of particles (NP)</td>
<td>100</td>
</tr>
<tr>
<td>Size of the external archive (SAR)</td>
<td>25</td>
</tr>
<tr>
<td>Weight damping rate (Wdamp)</td>
<td>0.99</td>
</tr>
<tr>
<td>Weight factor (w)</td>
<td>0.5</td>
</tr>
<tr>
<td>Acceleration coefficient</td>
<td>1</td>
</tr>
<tr>
<td>Acceleration coefficient</td>
<td>2</td>
</tr>
<tr>
<td>Number of grids per dimension (NGrid)</td>
<td>7</td>
</tr>
<tr>
<td>Inflation rate (α)</td>
<td>0.1</td>
</tr>
<tr>
<td>Leader selection pressure (β)</td>
<td>2</td>
</tr>
<tr>
<td>Deletion selection pressure (γ)</td>
<td>2</td>
</tr>
<tr>
<td>Mutation rate (μ)</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Figure 3. Pareto front of multi-objective test functions Pareto front of (a) ZDT1, (b) ZDT2, and (c) ZDT3

4. APPLICATION EXAMPLE: LOW NOISE AMPLIFIER DESIGN

4.1. Low noise amplifier circuit topology and analysis

The cascode topology with inductive source degeneration is the most widely used low-noise amplifier because it can simultaneously satisfy requirements for voltage gain and noise figure [29]. Figure 4(a) depicts the CMOS source inductive degeneration LNA topology, which uses inductive source
degeneracy to represent an inductor (Ld) connected to the source of the M1 transistor. The cascading (M2) transistor minimizes the effect between the tuned output and input. The biasing circuit is implemented using an M3 transistor connected as a diode. Figure 4(b) illustrates the small-signal circuit of an LNA cascode amplifier, which is used for analyzing noise, including an intrinsic transistor noise model. The input matching network, represented by an inductor (Ls), determines the input impedance of the LNA. To maximize the output power transfer, the output inductor Ld is used to resonate with the output load [30].

![Schematic and Small Signal Equivalent Circuit](image)

(a)

(b)

Figure 4. CMOS LNA Schematic and Small Signal Equivalent Circuit (a) CMOS LNA schematic and (b) LNA small signal equivalent circuit

4.1.1. Noise figure of the used low noise amplifier circuit

The definition of noise factor is defined by the following equation:

$$F = \frac{\text{Total output noise power}}{\text{Output noise due to the input source}}$$

In order to determine the expression for noise figure, it is necessary to apply thermal noise theory analysis to identify four distinct noise sources. Subsequently, the impact of these four sources on the output noise power must be determined using small signal analysis. The impact of the common-gate transistor on noise and frequency response is disregarded, along with the parasitic resistances of its D, S, G, and B terminals [31], [32]. In this noise analysis, four sources of noise have been considered: i) the thermal noise of the source resistance ($\tilde{i}_{n,RS}$); ii) the thermal noise of the output resistance ($\tilde{i}_{n,ROut}$); iii) the gate noise ($\tilde{i}_{n,G}$); iv) the channel thermal noise ($\tilde{i}_{n,d}$).

The impact of the cascode $M2$ transistor on the noise is insignificant when compared to the main $M1$ transistor. Furthermore, the noise from the MOSFET's source and bulk resistance is considered minimal and not taken into account for this analysis, as stated in references [33], [34]. The analysis focuses on the four primary noise sources that affect the output, namely $\tilde{G}_{o,RS}$, $\tilde{G}_{o,d}$, $\tilde{G}_{o,G}$, $\tilde{G}_{o,ROut}$ respectively [35]. The noise sources expressions are summarized in Table 3.
Table 3. Noise sources and output referred expressions

<table>
<thead>
<tr>
<th>Noise source</th>
<th>Expression</th>
<th>Output referred expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_s</td>
<td>( i_{n,rs}^2 = 4kT \frac{1}{R_s} \Delta f )</td>
<td>( i_{n,rs} = \frac{g_m}{(2Q \omega_0 C_{tot})} i_{n,rs} )</td>
</tr>
<tr>
<td>i_{n,d}</td>
<td>( i_{n,d}^2 = 4kT \beta g_{ds} \Delta f )</td>
<td>( i_{n,d} = -\frac{1}{2} i_{n,d} )</td>
</tr>
<tr>
<td>i_{n,g}</td>
<td>( i_{n,g}^2 = 4kT \gamma g_{ds} \Delta f )</td>
<td>( i_{n,g} = \frac{g_m}{(2Q \omega_0 C_{tot})} (1 - jR_s \omega_0 C_{tot}) / j2R_s \omega_0 C_{tot} i_{n,g} )</td>
</tr>
<tr>
<td>R_out</td>
<td>( i_{n,\text{route}}^2 = 4kT \frac{1}{R_{\text{out}}} \Delta f )</td>
<td>( i_{n,\text{route}} = i_{n,\text{route}} )</td>
</tr>
<tr>
<td>Correlation btw ( i_{n,d} ) and ( i_{n,g} )</td>
<td>( i_{n,\text{corr}}^2 = \frac{g_m}{(2Q \omega_0 C_{tot})} \frac{\Delta f}{\omega_0} i_{n,d} i_{n,g} )</td>
<td></td>
</tr>
</tbody>
</table>

As a result, the LNA noise factor is expressed as (9):

\[
F = \frac{i_{n,\text{rs}}^2 + i_{n,d}^2 + i_{n,g}^2 + i_{n,\text{corr}}^2 + i_{n,\text{route}}^2}{i_{n,\text{rs}}^2} \tag{9}
\]

Using the equations listed in Table 3, the noise factor at the resonance is obtained as (10):

\[
F = 1 + \frac{A + B + C + D}{E} \tag{10}
\]

Where,

\[
A = \left(\frac{1}{4}\right) \gamma g_{d0} \tag{11}
\]

\[
B = g_m^2 \left(\frac{C_{gs}}{C_{tot}}\right)^2 \left(Q^2 + \frac{1}{4}\right) \beta / (5 \gamma g_{d0}) \tag{12}
\]

\[
C = g_m \gamma C \left(\frac{C_{gs}}{C_{tot}}\right) \sqrt{\frac{\gamma \beta}{20}} \tag{13}
\]

\[
D = \frac{1}{R_s} \tag{14}
\]

\[
E = g_m^2 R_s Q^2 \tag{15}
\]

With the white noise factor, intrinsic gate capacitance, correlation coefficient, gate noise parameter, and the sum of Cgs, Cd, and parasitic capacitance are represented by, \( \gamma, C_{gs}, c, \beta, \) and Ctot, respectively.

The following equations provide the input quality factor Q at the resonance frequency \( \omega_0 \) :

\[
Q = \frac{1}{R_{\text{tot}} \omega_0 C_{\text{tot}}} \tag{16}
\]

Where,

\[
\omega_0 = \frac{1}{\sqrt{C_{\text{tot}}} C_{\text{tot}}} \text{ and } R_{\text{z}} = \frac{g_m L_z}{C_{\text{tot}}} \tag{17}
\]

The \( g_m \) and \( g_{d0} \) are approximated by the following expression [36].

\[
g_m = A_0 L A_1 W A_2 I_d A_3 \tag{18}
\]

\[
g_{d0} = B_0 L B_1 W B_2 I_d B_3 \tag{19}
\]

The length, width, and drain current of MOSFET transistors are represented by L, W, and Id, respectively. \( A_0=0.0423, A_1=-0.4578, A_2=0.5275, A_3=0.4725, B_0=0.0091, B_1=0.5637, B_2=0.5305, B_3=0.4695, \gamma=1.05 \) and \( \beta=3.8 \) are constants. Finally, the noise figure expression is given as follows:

\[
NF = 10 \log_{10}(F) \tag{20}
\]

4.1.2. Voltage gain of the low noise amplifier

The first stage provides the input impedance \( Z_{\text{in}} \) of this architecture at the resonance, Figure 4(b):
\[ Z_{IN} = j\omega (L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \]  

(21)

Where the input resistance is given by:

\[ R_{in} = Re[Z_{in}] = \frac{g_m}{C_{gs}} L_s \]  

(22)

And at the resonance frequency,

\[ \omega^2 = (L_g + L_s) C_{gs} = 1 \]  

(23)

The gain of LNA is given by the following equation:

\[ Gain = \frac{V_{out}}{V_{in}} = \frac{-j\omega g_m L_d}{1 - j\omega^2 C_{gs}(L_g + L_s) + j\omega g_m L_s} \]  

(24)

Substitute (23) into (24):

\[ Gain = \frac{V_{out}}{V_{in}} = \frac{-j\omega g_m L_d}{j\omega g_m L_s} = \frac{-L_d}{L_s} \]  

(25)

Where, the gate input inductor, the inductor source degeneration, the operating frequency, the transconductance, the source resistance and gate-source capacitance of M1 transistor, are represented by \( L_s, L_g, \omega_0, g_m, R_s \) and \( C_{gs} \), respectively.

4.2. Low noise amplifier design method

The problem of sizing ICs is addressed through multi-objective optimization algorithms and a performance evaluator based on analytical equations. The optimization process generates new sets of design variables at each iteration, including the width and length of transistors, as well as the sizes of resistors, capacitors, inductors, and other components [37]. The design methodology used is described in Figure 5. Two objective functions, namely the voltage gain and noise figure of an LNA circuit, are optimized using MOABC and MOPSO optimization techniques. The voltage gain should be maximized, and the noise figure should be minimized to obtain a good trade-off while respecting the design constraints and target specifications [38], as shown in Table 4.

![Figure 5. Flow diagram of LNA design method](image-url)
Table 4. LNA specifications design

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS 180 nm</td>
</tr>
<tr>
<td>Power supply (Vdd)</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Bias current (I&lt;sub&gt;d&lt;/sub&gt;)</td>
<td>&lt;8 mA</td>
</tr>
<tr>
<td>Power dissipation (Pd)</td>
<td>&lt;=15 mw</td>
</tr>
<tr>
<td>Operating frequency (F)</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Noise figure (NF)</td>
<td>&lt;3 dB</td>
</tr>
<tr>
<td>Voltage gain (S&lt;sub&gt;21&lt;/sub&gt;)</td>
<td>&gt;=10 dB</td>
</tr>
</tbody>
</table>

5. OPTIMIZATION AND SIMULATION RESULTS AND DISCUSSION

5.1. Optimization results using MATLAB

The MOABC and MOPSO algorithms are applied to simultaneously optimize two objective functions of the LNA circuit: the voltage gains and noise figure. Therefore, the main goal is to minimize the noise figure (NF) and maximize the voltage gain to achieve a good trade-off. Both algorithms have been applied to generate the Pareto front, shown in Figure 6. Table 5 shows three random solutions chosen from the archive of results obtained by the MOABC and the MOPSO algorithms.

Table 5. Optimization results

<table>
<thead>
<tr>
<th>MOABC algorithm</th>
<th>Solutions</th>
<th>W (um)</th>
<th>L (um)</th>
<th>I (mA)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol@1</td>
<td>49.877</td>
<td>0.215</td>
<td></td>
<td>07.780</td>
<td>16.841</td>
<td>0.785</td>
</tr>
<tr>
<td>Sol@2</td>
<td>50.000</td>
<td>0.220</td>
<td></td>
<td>06.137</td>
<td>15.593</td>
<td>0.906</td>
</tr>
<tr>
<td>Sol@3</td>
<td>50.000</td>
<td>0.198</td>
<td></td>
<td>10.000</td>
<td>18.901</td>
<td>0.968</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MOPSO algorithm</th>
<th>Solutions</th>
<th>W (um)</th>
<th>L (um)</th>
<th>I (mA)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sol@1</td>
<td>48.653</td>
<td>0.214</td>
<td></td>
<td>3.83</td>
<td>14.125</td>
<td>0.740</td>
</tr>
<tr>
<td>Sol@3</td>
<td>46.511</td>
<td>0.209</td>
<td></td>
<td>3.95</td>
<td>14.730</td>
<td>0.692</td>
</tr>
<tr>
<td>Sol@4</td>
<td>47.566</td>
<td>0.198</td>
<td></td>
<td>3.17</td>
<td>14.437</td>
<td>0.731</td>
</tr>
</tbody>
</table>

Figure 6. Pareto front of NF as function of gain and W

5.2. Simulation results using advance design system

The ADS simulator is used to simulate the low-noise amplifier circuit to verify the required design performances and specifications. The resulting values obtained by the MOABC and MOPSO algorithms are applied as the design circuit parameters in the ADS simulator. The simulations are performed using CMOS 180 nm process with a 1.8 V power supply. Figures 7 and 8 show the LNA test bench and simulation results of voltage gain and noise figure as functions of frequency, respectively.
Multi-objective optimization of CMOS low noise amplifier through nature-inspired ... (Hamid Bouali)

Figure 7. LNA test bench circuit

Figure 8. Simulation results of NF and gain as function of frequency of 3 solutions (sol@1, sol@2, sol@3)
Table 6 provides insights into the relative errors of the voltage gain and noise figure for two objective functions. The results suggest that the MOABC algorithm delivered the best trade-off solution (Sol@3) with the highest level of consistency between optimization and simulation outcomes. Furthermore, the MOABC algorithm’s performance surpassed that of the MOPSO algorithm, as evidenced by the lower relative error values of 22.22% and 29.91%, respectively. Table 7 shows a comparison of the optimization results obtained by the MOABC and the MOPSO techniques and by the other ones reported in the literature [39]–[43]. Therefore, we can notice that the obtained LNA design has a low noise figure and a high voltage gain, compared to other techniques documented in literature.

<table>
<thead>
<tr>
<th>Methods</th>
<th>Power supply (V)</th>
<th>Frequency (GHz)</th>
<th>Voltage gain (dB)</th>
<th>Noise figure (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACO</td>
<td>2.3</td>
<td>2.4</td>
<td>9.432</td>
<td>0.328</td>
</tr>
<tr>
<td>ACO</td>
<td>2.3</td>
<td>2.4</td>
<td>10.24</td>
<td>0.310</td>
</tr>
<tr>
<td>Classic</td>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>3.4</td>
</tr>
<tr>
<td>Classic</td>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>3.2</td>
</tr>
<tr>
<td>Classic</td>
<td>1</td>
<td>2</td>
<td>1.2</td>
<td>5.6</td>
</tr>
<tr>
<td>GA</td>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>0.745</td>
</tr>
<tr>
<td>MOPSO</td>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>0.731</td>
</tr>
<tr>
<td>MOABC</td>
<td>2</td>
<td>2</td>
<td>1.8</td>
<td>0.816</td>
</tr>
</tbody>
</table>

6. CONCLUSION

In this paper, we have presented an optimization approach for the optimal sizing of an LNA circuit. The proposed MOABC and MOPSO algorithms were adapted and successfully applied to maximize the voltage gain while minimizing the noise figure of the LNA circuit. The optimized design, implemented in a CMOS 180 nm process, operates at 2.4 GHz with a 1.8 V power supply. The proposed circuit design achieves a better trade-off between voltage gain and noise figure (Gain=21.200, NF=0.848) while consuming less power. The optimized designs were simulated using the ADS simulator to verify the validity of the results achieved by the algorithms. The optimization and simulation values were in agreement, showing the benefits of the proposed design methodology. The results are very promising for helping the designers reduce the number of redesign iterations by only selecting the best design for a specific application. Finally, the achieved LNA design shows better performance than other optimization-based methods previously reported in the literature.

REFERENCES


Bulletin of Electr Eng & Inf, Vol. 12, No. 5, October 2023: 2824-2836
Multi-objective optimization of CMOS low noise amplifier through nature-inspired … (Hamid Bouali)


**BIOGRAPHIES OF AUTHORS**

**Hamid Bouali** received a B.A. degree in electronics from the faculty of sciences of Moulay Ismail University, Meknes, Morocco and a master’s degree in Microelectronics from Faculty of Science Dhar El Mahrez of Sidi Mohamed Ben Abdellah University, Fez, Morocco. He has more than 6 years experience in Analog Integrated Circuits layout. He is currently a Ph.D student in department of physics. His research interests are related to design and optimization of ICs area using swarm intelligence techniques. He can be contacted at email: ham.bouali@edu.umi.ac.ma.

**Prof. Dr. Bachir Benhala** received a master’s degree in Telecommunication Systems and Micro-electronic, a Ph.D degree in Electronic and Micro-electronic, from the Faculty of Science and Technology of Fez, Morocco. He has more than 6 years experience in Analog Integrated Circuits layout. He is full Professor at Sidi Mohamed Ben Abdellah University in Fez, Morocco. His research interests include analog design automation, digital/analog VLSI architecture, telecommunication and RF circuits, embedded systems, signal processing, applied optimization techniques. He can be contacted at email: bachir.benhala@usmba.ac.ma.

**Mohammed Guerbaoui** is a Professor of Electrical Engineering and member of Modelling, Materials and Control of Systems team at Laboratory of Computer Engineering and Intelligent Electric Systems in the Higher School of Technology, Moulay Ismail University, Meknes, Morocco. He received the Ph.D. degree in 2014, from Faculty of Sciences, Moulay Ismail University, Meknes. His research interests are mainly focussed on power quality, electrical drives, fuzzy logic control techniques for greenhouse drip irrigation. He can be contacted at email: m.guerbaoui@est.umi.ac.ma.