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CMOS low noise amplifier technologies: trends for enhancing satellite receivers and mobile communications

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ABSTRACT

The emerging demand for high-data-rate wireless communication systems and high-resolution radars, particularly in the millimeter-wave (mm-wave) spectrum, has captured significant attention within both the industrial and academic landscape. Recognized as the fundamental building block for satellite receivers, the low noise amplifier (LNA) plays a pivotal role in meeting these growing requirements. In Today's world a continuously increasing number of connected devices and resource-intensive digital content load to an incessant data being generated, transformed, and facilitated. In this paper, authors summarize the different technologies and techniques employed to design various LNAs with enhanced bandwidth, higher gain, low noise figure (NF), minimal power consumption, and less chip area.

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1. INTRODUCTION

In recent, the utilization of wideband amplifiers has been known across various domains, encompassing satellite receivers, medical instruments, electronic devices, radio communication systems, mobile communication devices, radio astronomy setups, cryogenic systems, Bluetooth technology, and global positioning system (GPS) systems [1]-[10]. A crucial component in these amplification systems is the low noise amplifier (LNA), specifically engineered to augment signals with minimal power consumption, while preserving the signal-to-noise ratio (SNR) [11]-[20]. Distinguishing itself as the sole amplifier capable of enhancing both signal and noise power, LNAs play a pivotal role in mitigating additional noise within the signal. The application spectrum of LNAs spans satellite receivers, medical instruments, electronic devices, radio communication systems, and mobile communication devices [21]-[28].

A good LNA is characterized by a low noise figure (NF), sufficient gain to amplify the signal adequately, and a high inter-modulation and compression point to fulfill its intended function. The utilization of LNAs in satellite communication systems is necessitated by the imperative to amplify exceedingly weak signals received from satellites [20]-[25]. The inherent weakness of these signals arises from the considerable distances they traverse, underscoring the need for amplification. Moreover, the power resources on satellites are constrained, precluding the use of conventional amplifiers that introduce noise potentially masking the genuine signal. Consequently, designers opt for LNAs that exhibit reduced inductors, and capacitors and employ low-noise (LN) transistors. Unlike conventional amplifiers, which amplify both the signal and accompanying noise, LNAs are designed to reduce additional noise and also keep the signal quality high [20]-[30]. Despite versatile applications in the satellite receiver, medical instruments, electronic

equipment, radio communication, mobile communication, blue tooth technology, and GPS, these LNAs are faced with drawbacks such as achieving high gain-bandwidth, reducing NF, high power consumptions, heating issues, and increase in the size of the chip [20]-[40].

Currently, different technologies such as complementary metal-oxide-semiconductor (CMOS), heterojunction bipolar transistor (HBT), and high electron-mobility transistor (HEMT) are employed to achieve desirable features in the design of LNAs for their applications in satellite receivers and mobile communications [40]-[45]. The HBT is denoted as a specialized type of bipolar junction transistor (BJT) displaying the ability to form a hetero-junction. This unique design advocates the utilization of distinct semiconductor materials for the emitter and base junctions. Such transistors are extensively employed in contemporary ultrafast circuits, particularly in radio frequency (RF) systems, as well as in applications emphasizing high power efficiency, such as RF power amplifiers in cellular phones [45]-[51].

HEMT devices exhibit superior operational capabilities at elevated frequencies when compared to alternative transistor technologies. The spectrum of HEMT applications spans satellite receivers, low-power (LP) amplifiers, and cellular communication devices. Key advantages associated with HEMT technology encompass heightened gain, rapid switching speeds, and diminished noise levels [52]-[55].

A buffer layer is used between two materials with different lattice constants in the case of metamorphic HEMT (mHEMT). This is the improvement of pHEMT. The buffer layer is typically made of ALLnAs. This configuration provides high gain and LN [56]-[58].

To design CMOS LNAs, there are reports using different techniques such as inductive series peaking, resonator coupling technique, gain boosting, double transformer-coupling, dual channel-shunt, and impedance matching for achieving better features such as small chip size, low NF, low power consumption, and high gain [28]-[51]. This paper summarizes the recent knowledge and status on the use of various technologies and techniques for designing CMOS LNAs for dedicated applications in satellite receivers and mobile communications, sensor management, event detection, sensor information fusion, and multi-hop communication. This review paper emphasizes the relevance of wideband amplifiers that spans diverse fields, including satellite receivers, medical instruments, electronic devices, and communication systems like radio and mobile.

2. BASIC OF LOW NOISE AMPLIFIER

The LNA is designated as the primary component in the initial stages of receiver design. It is proposed that the LNA significantly contributes to enhancing the performance, particularly the sensitivity, of wireless communication systems. The utilization of the cascode architecture has been recommended to achieve a substantial level of isolation between the input and output stages. Subsequently, transistor M2 serves to isolate the Miller capacitance from other components, thus enhancing the overall performance [1]-[10]. In this schematic model, the input impedance is demonstrated to be derived through the incorporation of the source degeneration inductor Ls. Additionally, the gate inductor Lg is introduced to initiate frequency resonance. Furthermore, within the same schematic model, tuning granularity is achieved through a network involving a matching output composed of a varactor and a satellite. The load impedance is then transformed into a single parameter for the subsequent stage, acting as the input impedance through the utilization of an LC network [15]-[20].

When the matching network is well-designed, it helps send the most power to the load. Changing the input voltage to the varactor (DC) makes the output frequency match a different frequency. The basic architecture of the LNA is depicted in Figure 1 [1]-[20].

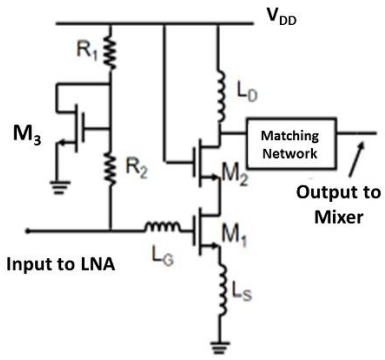

Figure 1. Basic architecture of LNA

3. CMOS LOW NOISE AMPLIFIER

To reduce the degradation of the SNR, numerous studies advocate the incorporation of high gain and a minimal low NF in the initial stage component of the RF receiver designed for ultra-wideband (UWB) systems [1]-[20]. Moreover, the importance of high gain and low NF in the LNA has been underscored, considering that the noise characteristics of the RF receiver's front end are determined by the LNA. It is noteworthy that designing effective wideband LNAs necessitates key attributes such as a flat and wideband gain, elevated gain levels, and a low NF, especially across the entire UWB frequency band, while also minimizing power consumption [20]-[30].

Concerning the integration of an antenna port, the recommendation is for a wideband 50 Ω input matching. Although three main methods for achieving wideband matching exist, the described topologies encounter challenges, including high NF in the resistive termination and common gate configurations, as well as a large chip area in the bandpass LC filter configuration [20]-[30]. In the current context, a preference for the calculation of a two-frequency matching method has emerged as a means to attain wideband input matching while circumventing the drawbacks associated with the aforementioned LNAs.

Recent research efforts have delved into novel circuit topologies for wideband LNAs, such as resistive shunt feedback topologies and distributed topologies. These studies have demonstrated significant relevance owing to their enhanced wideband characteristics. Notably, resistive shunt feedback amplifiers have been identified as capable of achieving appreciable wideband input matching and gain [30]-[40]. Given applications and scope of improvement in LNA, a broadband LNA is reported which is transformer-based and used in mm-wave applications. The authors use four common source stages and the circuit is implemented on a 65-nm CMOS process showing a gain of 17.7 dB, NF value 5.4-7.4, and achieved chip area of 0.37 mm^2 [1]. There is another report to design an mm-wave LNA in a 28-nm fully-depleted (FDSOI) CMOS technology. This LNA shows the total power consumption of 38.2 mW with a gain over 12 dB from 53 to 117 GHz, and recorded an NF of 6 dB from 75 to 105 GHz [2].

In line with the above applications, an E-band transmitter is implemented which is wideband and high linearity and implemented on 55-nm silicon-germanium (SiGe) bipolar (BiCMOS) technology. The circuit encompasses a double-balanced bipolar ring mixer and broadband power amplifier which uses a 2-way output power combined with an integrated low loss balun transformers. This circuit denotes a conversion gain of 24 dB and 22 dB, output power of 16.8 dBm, and power consumption-575 mW [3]. Another approach to improve the designing of 60-GHz broadband heterodyne LNA is performed using the low-coupling coefficient transformer-based matching network and the tail switch technique. The designed LNA shows a 20-to-75-dB conversion gain, a 5-dB NF which is fabricated in a 65-nm CMOS with a chip area of 1.9×0.7 mm [4]. Another design of two-stage 60-GHz LNA is reported in a 28-nm LP bulk CMOS process. The obtained circuit shows a power gain value of 13.8 dB, bandwidth of 18 GHz, 4 dB NF value, and power consumption of 24 mW of DC power [5]. Additional data is reported from CMOS LNA designed in a 65 nm node. The designed circuit is shown to consume 78 mW and occupies 1.4 mm^2 of active chip area and measures a value of 30.5 dB gain and 6.7 dB NF [6]. Another three-stage single-ended LNA in 90 nm CMOS technology reports a peak gain of 14 dB and a low NF value of 4.8 dB. This circuit also shows an increase of 3 dB bandwidth, power consumption of 32 mW, and chip area of 0.065 mm^2 [15]. There is a report on an ultra-LP 60 GHz LNA in a 90 nm CMOS technology that records a 12.5 dB peak gain and a low NF of 5.4 dB in a 90 nm CMOS technology. The suggested LNA measures a power consumption of 4.4 mW from a 1 V supply with a chip area of 0.047 [16].

In summary, the importance of SNR in RF receivers, particularly in UWB systems is of paramount importance. There is aneed on the significance of incorporating high gain and low NF in the initial stage of the RF receiver, with a focus on the design of wideband LNAs. These LNAs are crucial for applications in mm-wave and E-band transmitters, with efforts directed towards achieving wideband input matching and improved performance metrics.

4. DESIGN OF CMOS LNA WITH DIFFERENT TECHNIQUES

Currently, the design of CMOS-based LNAs is supported with various techniques such as inductive series peaking, current reuse topology, common-gate (CG) topology, dual resonance network, and transformer feedback Gm-boosting magnetic coupled techniques [29]-[51]. To exploit various technologies and be supported with techniques, wideband LNAs are designed and fabricated in a CMOS multi-cascode process and supported with a noise-reduction transformer topology. By using the discussed topology method, the Q-band LNA reports a gain of 20.3 dB and an NF of 4.6 dB at 40 GHz, with a power consumption of 15 mW [29]. Another topology-based broadband LNA is reported by using T-type matching topology in 0.25-μm and 0.13-μm SiGe BiCMOS technologies. The proposed LNA shows a high gain of about 23 dB and an NF value of less than 7.2 dB (from 50 to 75 GHz) for the V-band LNA and below 7 dB (from 78 to 110 GHz) for the W/F-band LNA [30]. There is another report on a LP and high power-gain (S21) ultraviolet B (UVB) PNA

implemented on 0.13-µm CMOS technology. In this paper, the load effect of CG topology is employed in combination with a dual-resonance load network for both wideband input matching and NF flatness.

Here, the LNA circuit shows the high and flat power gain of 13.5±1.5 dB including input return loss better than 13 dB and a flat NF of 4.3 dB ±0.4 dB for frequencies 3–12 GHz. This reported LNA shows a die area of 1.09 0.8 mm^2 including pads and a value of power consumption of 8.5 mW from a 1.2-V DC supply [35]. Next, the authors suggest a design of a LP, high-gain, and low NF CMOS distributed amplifier consuming a cascaded gain cell and designed encompassing inductively parallel-peaking cascode-stage. The authors elucidate that the two-stage distributed amplifier (DA) can consume 22 mW and achieve flat and high of 14.07 1.69 dB combining average NF of 2.8 dB spread to the 3–10-GHz band with a preferred range [36].

There is a report on designing a channel-selecting low-noise amplifier (CS-LNA) which has blocker filtering capability and is implemented in 32-nm CMOS SOI. This design is specified for SAW-less diversity path receiver (RX), this receiver is applied in frequency division duplexing (FDD) cellular system. Authors use a filter feedback network to avoid leakage and improve out-of-band (OOB) input-referred third-order intercept point (IIP3) [33]. A wideband LNA which is implemented in 0.18- m CMOS technology. Data show that the proposed LNA achieved power gain of greater than 10 dB input return loss is below 10 dB from 2 to 11.5 GHz and NF ranges from 3.1 to 4.1 dB over the band of interest. In this paper, the ratio of figure-of merit to chip size is shown as high as 190 (mW 1 mm^2) [34].

There is a report on the fine-tuning of dual feedback LNA using the novel power-detection-based automatic frequency calibration technique in 65-nm CMOS technology. In this approach, authors find that designed LNA can possess 95–105-dB high conversion gain and 1.7–8-dB NF over 0.1–5 GHz frequency range [41]. Further, an LNA is reported to be fabricated in a 40-nm CMOS process at three stages and coupled with double-tuned transformer techniques. This LNA shows 18–26 dB gain and 3.3–4.3 dB NF concurrently with a power consumption value of 21.5–31.4 mW across a 26–33 GHz frequency range [42]. Another attempt to design an LNA is reported in 65 nm CMOS technology using a resistive-feedback network and inductive-series peaking technique. This approach of designing LNA in cascaded three-stage confers a power gain of 8 dB and NF in the range of 4.5 to 6.8 dB for a frequency range of 2.1–39 GHz [43]. Additionally, a report on the design of a D-band LNA using gain boosting in a 0.13 SiGe BiCMOS technology includes two stages of cascode amplifiers. Data show that power gain of more than 20 dB gain from 110 to 140 GHz, low power use of 12 mW of total DC and NF value is in the range of 5.5 to 6.5 dB [44].

A wideband LNA is reported in 0.18-m CMOS technology with shunt resistive feedback and series inductive-peaking technique. Here, the authors suggest that the proposed LNA can have a power gain of more than 10 dB and the NF varies from 3.1 to 4.1 dB in a particular band [45]. Further, an LNA circuit is created using a dual resonance network and coupled with an inductive series peaking technique. This LNA is shown to acquire the high and flat power gain of 13.5±1.5 dB and a flat NF of 4.3 dB ±0.4 dB at 3–12 GHz [46]. Lin and Chang [47] report on a LN CMOS DA using inductively series-peaking cascaded gain cell with the two-stage. This CMOS DA demonstrates power consumption of 22 mW and achieves a flat and high gain of 14.07 1.69 dB with an average NF value of 2.8 dB in the range of 3–10-GHz band [47]. Another important LNA design presents two CMOS CG LNAs with different dual-feedback techniques and they find an appreciable reduction in the NF value up to around 2 dB [48].

Another key LNA is reported to be used in multi-standard mobile broadcast receiver employing novel wideband impedance matching technique. In this reported LNA, authors find a voltage gain of 25 dB and NF of 1.6 dB [49]. An LNA design using a new dual-channel shunt technique and inductive-series peaking is reported. In this case, LNA is in the 0.18 µm CMOS process and indicates a high power gain of 10.2 dB and NF value ranged from 3.9 to 4.5 dB [50]. Another paper reports on the design of LNA in 65 nm CMOS technology employing a double-transformer-coupling technique. In this paper, the authors show that. Three-stage LNA can achieve a peak gain of 31.4 dB, a low NF value of 4.7 dB, and a low power consumption of 6 mW [32], [51]. Taken together, there is a need to understand and critically review various techniques and technologies used in the design of CMOS-based LNAs, aiming to achieve specific performance metrics such as gain, NF, and power consumption. These techniques include inductive series peaking, current reuse topology, CG topology, dual resonance network, and transformer feedback Gm-boosting magnetic coupled techniques. These LNAs are designed for a wide array of applications, including satellite receivers, communication systems, and medical instruments, highlighting the versatility and importance of LNAs in modern electronic devices and systems.

5. SUMMARY

In summary, various LNAs are reported for satellite receivers and mobile applications using different technologies and techniques showing unique achieved features like high gain, high bandwidth, low NF, reduced area, and minimal power consumption. These designs of LNAs keep current applications in the industry with advantages with selective and appropriate uses. Wideband amplifiers are used in various fields,

such as satellite receivers, medical instruments, and communication systems. A key component in these systems is the low noise amplifier (LNA), designed to enhance signals while minimizing power consumption and preserving the signal-to-noise ratio. LNAs are critical for applications requiring low noise, such as satellite communications, where they amplify weak signals without adding significant noise. Technologies like CMOS, HBT, and HEMT are employed to improve LNA performance, addressing challenges like high gain bandwidth and low power consumption. This paper reviews the latest advancements in LNA design for satellite receivers, mobile communications, and other applications. A summary of the comparison of LNAs presented in this paper is given Table 1.

Table 1. Comparison of achieved gain, bandwidth, NF, and area in LNAs designed using various technologies

Paper no.	Gain (dB)	Bandwidth (GHz)	Area (mm^2)	NF (dB)	Process/technologies	Stages
[1]	17.7	35.6	0.37	5.4-7	65 nm CMOS	4 stages
[2]	12	-	0.456	6	28 nm CMOS	3 stages
[4]	20	8.5	1.33	5	65 nm CMOS	3 stages
[33]	-	15	0.28	3.6-4.9	32 nm CMOS	3 stages
[34]	17.4	-	-	7.8	0.18 µm	3 stages
[35]	30	12.7	-	2-2.9	65 nm	3 stages
[36]	21.7	-	0.26	8.4-10.4	28 nm	3 stages
[38]	32.5	117	0.15	-	0.18 µm CMOS	4 stages
[40]	16.5	12	-	5.2	28 nm CMOS	-
[41]	95	20	5	1.7-8	65 nm CMOS	3 stages
[42]	27.1	7.4	0.26	3.3-4.3	40 nm CMOS	1 cascode 2 differential
[43]	11.5	-	0.16	4.5	65 nm CMOS	-
[52]	-	1.5	0.18	1-1.5	110 nm CMOS	-
[53]	17.0	9.0	0.293	7.6	22 nm FDSOI	-
[54]	13.04	-	0.17	4.47	65 nmCMOS	-
[55]	41.0	-	-	2.4	CMOS	-
[56]	-	2.4-9.4	-		0.18 µmCMOS	-
[57]	25	-	-	14	45 nm RFSOI	-
[58]	21.7	-	-	1.6	0.18 µm CMOS	-

6. CONCLUSION

The most common stage of LNA in which maximum work is done is three stages. CMOS is the basic building block of LNA but there are lots of techniques used in LNA like HBT, HEMT, and inductive series peaking. It is also concluded that if the number of stages is increased in LNA then NF is increased which can be decreased by applying improved techniques. Hence, newly designed LNAs encompassing features such as high gain, low NF, low power consumption, and less chip area could bring new avenues in the satellite receivers and mobile communications with better efficiency and suitability.

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